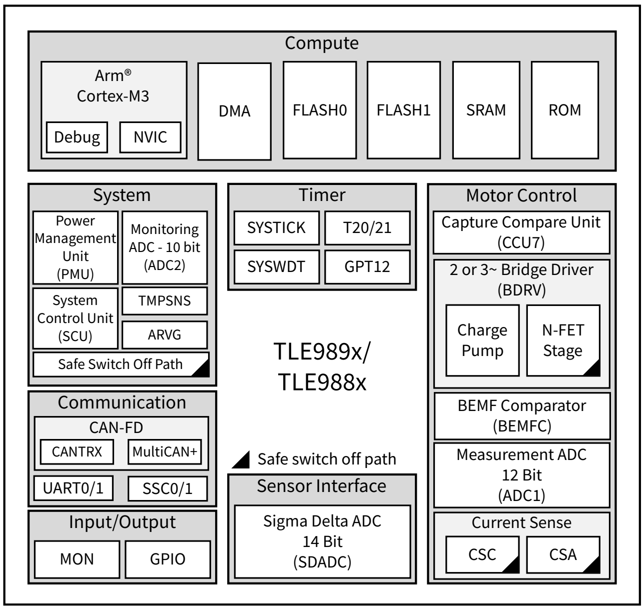
MOTIX™ TLE989x/TLE988x

Microcontroller with CAN-FD and NFET Driver for BLDC Applications
AK step

Features

- 32-bit Arm® Cortex®*-M3 core at up to 60 MHz
- Single power supply from 5.5 V to 28 V
- FLASH0 up to 32 KB, FLASH1 up to 256 KB with EEPROM emulation, RAM up to 32 KB
- 1x CAN-FD protocol handler and transceiver
- 2x UART (with LIN support), 2x SSC
- 3-phase bridge driver with charge pump and PWM generation (CCU7) and safe switch off path
- 1x low side shunt current sense amplifier and comparator
- 3x BEMF comparators
- 1x 12-bit ADC with 19 inputs and 1x 10-bit ADC with 14 inputs
- 14-bit SDADC with 2x2 differential inputs for rotary sensor measurement
- 12x 16-bit timer, 1x 24-bit timer (SYSTICK)
- 8/16 GPIOs (incl. RESET, SWD) and 7/10 GPIs (incl. XTALI/O), package dependent (TQFP-48/LQFP-64)
- Fail safe mechanism and error handling with safe switch off path for bridge driver (according to ISO26262 Safety Element out of Context for safety requirements up to ASIL-B)
- Security: Layered access right management, secured boot and key storage
- Temperature Range T_J: -40°C up to 175°C
- Ultra compact application footprint with packages TQFP-48 and LQFP-64



Potential applications

- Automotive motor control for auxiliary drives like pumps, fans, HVAC, actuators, sunroof

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100

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1 Overview

The TLE989x/TLE988x has following features:

- Arm® Cortex®-M3 core system
    - Up to 60 MHz CPU and system frequency
    - Arm® NVIC interrupt controller with 32 interrupt requests and 32 levels
    - Arm® Coresight debug with 2 hardware breakpoints and 2-wire interface (SWD)
    - Arm® µDMA direct memory access controller with 8 channels
    - Arm® SysTick system timer (24-bit)
- Single system power supply connected to battery supply (VS pin)
    - Operating range from 5.5 V to 28 V, extended operating range from 3 V to 40 V
    - Low-dropout voltage regulators (LDO) for pad and CAN supply (VDDP, VCAN) and core supply (VDDC)
    - 5 V low-dropout voltage regulator for on-board loads (VDDEXT)
- On-chip clock generation
    - Low power oscillators as clock source in startup and power saving modes, also used as independent safe watchdog timer clock
    - High precision oscillator as base and fallback clock source for system with clock watchdog
    - Oscillator circuit for external crystal/resonator for accurate clock source with clock watchdog
    - Two low jitter phase lock loop circuits (PLL0/1) with programmable prescaler for system clock with loss-of-lock detection and fallback clock
- Control state machine for switching the system states
    - Active mode: system fully operational with power saving options for frequency and peripherals; bridge driver in active mode, brake mode or off; current consumption typ. 20 mA at V_S (MCU and CAN active, bridge driver off)
    - Stop mode: MCU subsystem stopped with monitoring and communication peripherals listening
    - Sleep mode: MCU subsystem unpowered with wake monitoring active; wake-up time typ. 2 ms and typ. 30 µA at V_S
    - Wake capabilities for stop and sleep modes via cyclic timer event or CAN/MON event
- On-chip memory
    - Up to 256 KByte FLASH1 for non-volatile code and data storage with ECC
    - Up to 32 KByte FLASH0 for non-volatile code and data storage with ECC, EEPROM emulation support
    - 1024 Byte 100 Time Programmable Memory with ECC (100 TP)
    - Up to 32 KByte RAM with ECC
    - BootROM for startup firmware, bootstrap loader (BSL) and flash routines
    - Key storage for supporting security routines
- Security features
    - Secured boot mechanism as anchor for in-field software updates
    - CMAC and AES functions
    - Key storage with key management support
    - Layered access right management

- Communication features
  - MultiCAN+ protocol handler with CAN-FD support (up to 2 MBaud) and 32 message objects
  - CAN-FD transceiver compliant to ISO11898-2 and ISO11898-5 up to 5 MBaud
  - 2x full duplex asynchronous serial interface (UART0/1) with LIN support
  - 2x synchronous serial channel (SSC0/1) up to 30 MHz (master mode) and 15 MHz (slave mode)
- Wake-up capable high voltage monitoring input(s) (MONx) with input range of -28 V to 40 V (with series resistor)
- General-purpose I/O Ports (GPIO) with push-pull, open-drain and pull-up/down arrangement
  - TQFP-48: 8 GPIOs (incl. RESET, SWD)
  - LQFP-64: 16 GPIOs (incl. RESET, SWD)
- General-purpose input Ports (GPI) with pull-up/down arrangement
  - TQFP-48: 7 GPIs (incl. XTALI/O)
  - LQFP-64: 10 GPIs (incl. XTALI/O)
- Optimized functionality for BLDC motor control
  - 3-phase bridge driver for N-Channel MOSFETs with programmable current driven output stage, various diagnosis and protection features in on and off state. The bridge driver allows an EMC and thermally optimized switching behavior for MOSFETs of up to 6 x 150 nC at 20 kHz
  - 2-stage charge pump operating down to V_{SD} = 5.4 V allowing motor operation for wide supply range from V_S = 4.4 V to 28 V (cranking and load dump situation)
  - High speed current sense amplifier (CSA) for single shunt current measurement in ground path with programmable gain
  - Current sense comparator (CSC) with programmable threshold for fast overcurrent detection and safe switch off request
  - 12-bit ADC (ADC1) for measurement of eight high and ten middle voltage inputs with deterministic sample trigger, four time-triggered sequences and digital postprocessing
  - 3x BEMF comparators for sensorless block commutation
  - Capture/compare unit (CCU7) with five 16-bit timers for sophisticated 3-phase PWM pattern generation
- Sensor interface
  - 14-bit Sigma Delta ADC (SDADC) for rotary sensors with two differential channels supporting AMR/GMR/TMR type sensors
- General purpose timer
  - GPT12 (five 16-bit), Timer 20 (16 bit), Timer 21 (16 bit)
- Monitoring ADC
  - 10-bit ADC (ADC2) for background monitoring of five external and eight internal voltages with programmable threshold, warning flag indication, shut down and interrupt request
- Fail-safe mechanism and error handling
  - Power-on and undervoltage/brown-out reset generator
  - Supervision of all system supply voltages
  - Clock monitoring for master clock, external clock, system clock and PLL with error handling
  - Overtemperature detection sensing the junction temperature at two die locations with warning flag indication and automatic error handling
  - Drain source monitoring of bridge driver for detection of short circuit (in on/off state) and open load diagnosis (in off state)

  - All memories (flash and RAM) with single bit error correction and double bit correction (SECDET)
  - 2x window watchdog (FS_WDT and SYSWDT) with independent clock source
  - Safe switch off for bridge driver at severe system malfunction (FS_WDT overflow, shunt overcurrent, supply under-/overvoltage, failure input active) and failure indication according to ISO 26262 Safety Element out of Context for safety requirements up to ASIL-B
- Temperature range T_J: -40°C up to 175°C
- Packages TQFP-48 and LQFP-64
- Green package (RoHS compliant)
- AEC qualified (Grade 0)

2 Block diagram

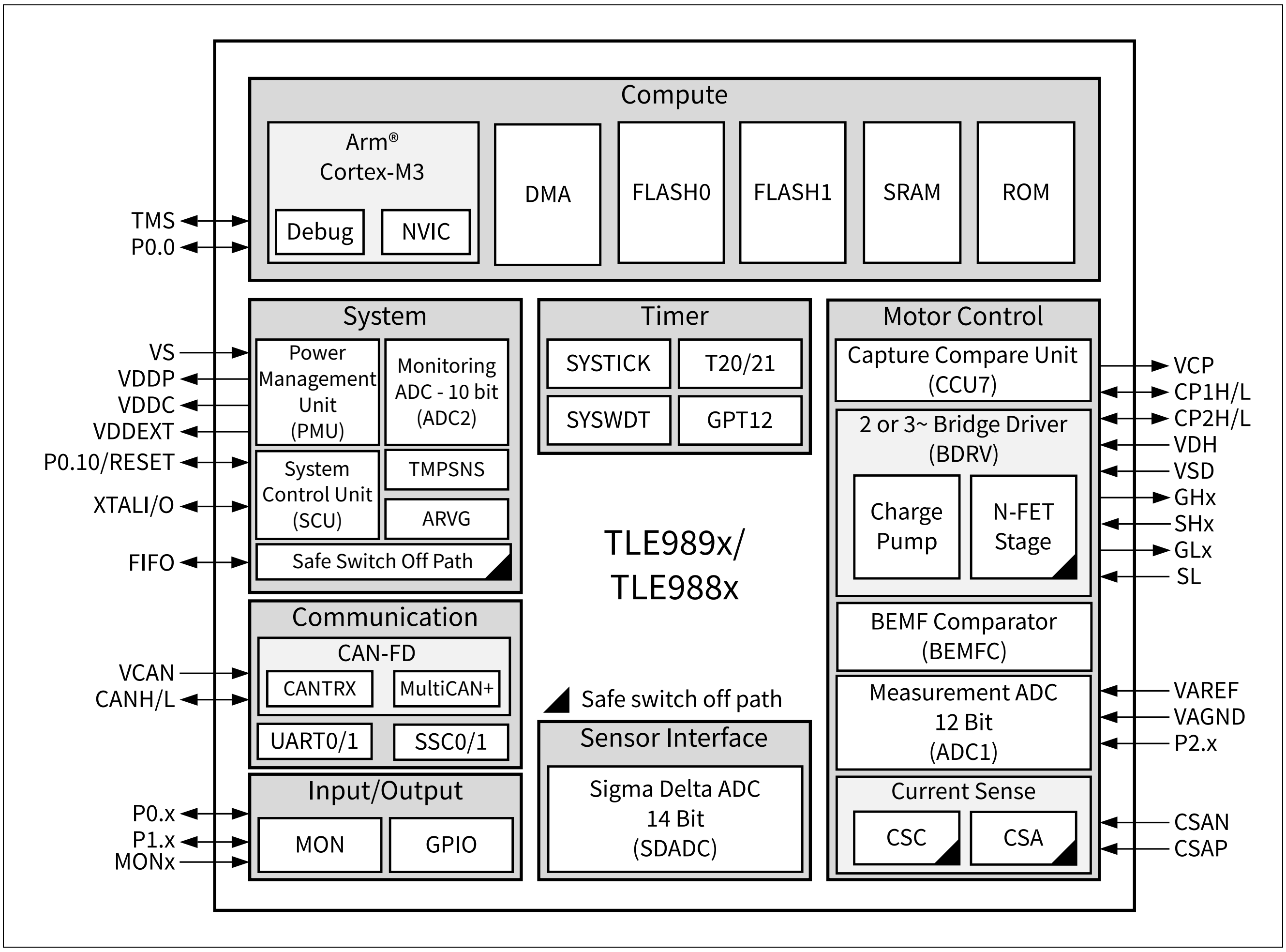


Figure 1 **Block diagram TLE989x/TLE988x**

3 Product definitions

3.1 Device pinout

3.1.1 Device pinout 48 pins

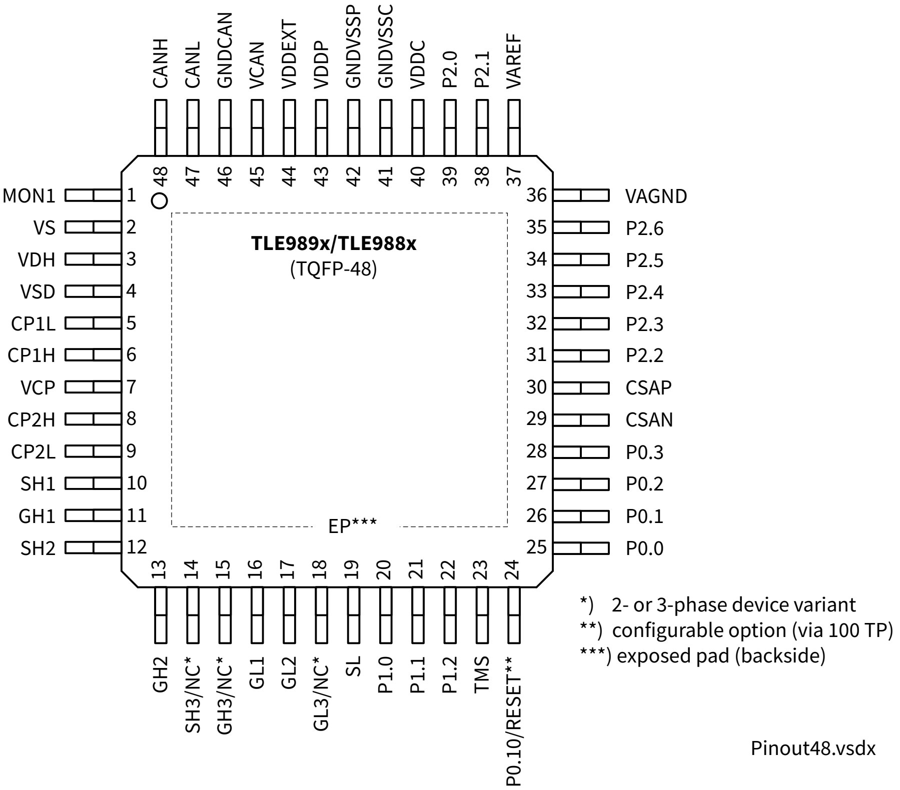


Figure 2 **Pinout for 48 pin package**

3.1.2 Device pinout 64 pins

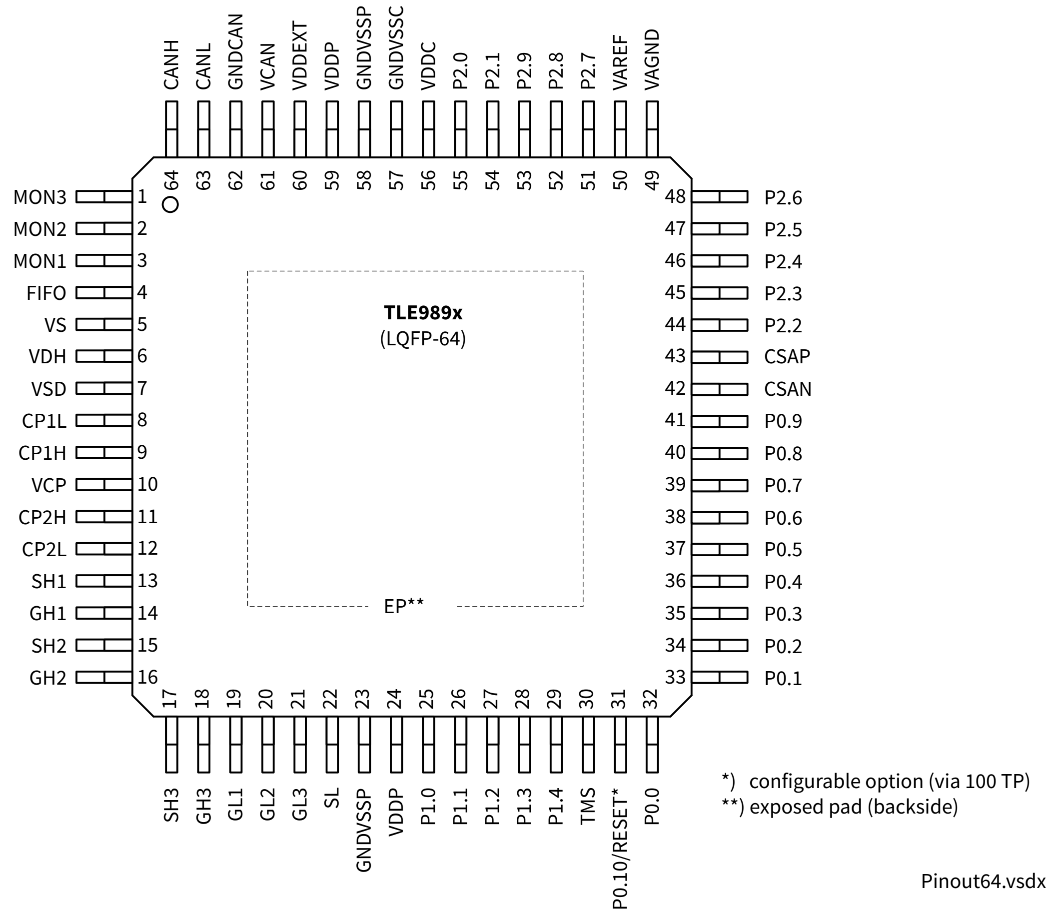


Figure 3 Pinout for 64 pin package

3.2 Device packages and ordering information

The device is offered in following package(s), see **Table 1**.

Table 1 Device packages

Name	Number of pins	Body size [mm²]	Pin pitch [mm]	Epad	Designed for automatic lead tip inspection (LTI)
TQFP-48	48	7 x 7	0.5	yes	yes
LQFP-64	64	10 x 10	0.5	yes	yes

Ordering information

This datasheet covers the products with different package markings. Each marking has a separate ordering number. The features of the different markings are described in **Table 2**.

Table 2 Ordering info

Marking	Package	FLASH1 [KB]	FLASH0/ EEPROM$_B$ [KB] 1)	RAM [KB]	Security [KB] 2)	CAN	SDADC	Functional safety
TLE989x Grade-0 (3 ph)								
TLE9893-2QKW62S	LQFP-64	248	24+8	31	8+1	CAN-FD	Yes	ASIL-B
TLE9893QKW62S	LQFP-64	248	24+8	31	8+1	CAN-FD	No	ASIL-B
TLE9893-2QTW62S	TQFP-48	248	24+8	31	8+1	CAN-FD	Yes	ASIL-B
TLE9891-2QTW61	TQFP-48	120	24+8	16	0	CAN-2.0	Yes	ASIL-B
TLE9891-2QTW60	TQFP-48	120	24+8	16	0	CAN-2.0	Yes	QM
TLE989x Grade-1 (3 ph)								
TLE9893-2QTA62S	TQFP-48	248	24+8	31	8+1	CAN-FD	Yes	ASIL-B
TLE9893-2QTA62	TQFP-48	248	24+8	31	0	CAN-FD	Yes	ASIL-B
TLE9891QTA61	TQFP-48	120	24+8	16	0	CAN-2.0	No	ASIL-B
TLE988x Grade-0 (2 ph)								
TLE9883-2QTW62S	TQFP-48	248	24+8	31	8+1	CAN-FD	Yes	ASIL-B
TLE9881-2QTW60	TQFP-48	120	24+8	16	0	CAN-2.0	Yes	QM
TLE988x Grade-1 (2 ph)								
TLE9883QTA62	TQFP-48	248	24+8	31	0	CAN-FD	No	ASIL-B

Notes

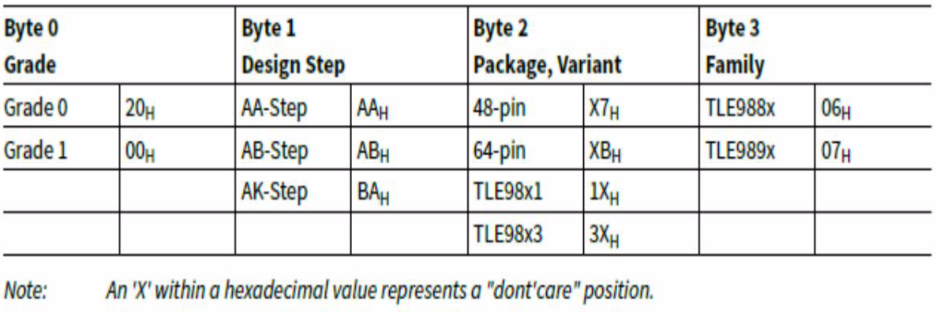
1. *The EEPROM is emulated in FLASH0 and allocates 8 KB, the remaining 24 KB are free for user functions.*
2. *The security functions allocate 8 KB of FLASH1 and 1 KB of RAM.*
3. *Functional safety term “ASIL-B” refers to “Safe Switch Off”, see also Safety Manual (Z8F63951407).*

JTAG ID

The JTAG ID of the TLE989x/TLE988x is 0x1021 F083.

Customer ID

The Customer ID contains the device specific variant information. It can be read using a firmware API routine, refer to the firmware user manual. The decoding of the Customer ID is described in the following figure.



Byte 0 **Grade**		**Byte 1** **Design Step**		**Byte 2** **Package, Variant**		**Byte 3** **Family**	
Grade 0	20_H	AA-Step	AA_H	48-pin	$X7_H$	TLE988x	06_H
Grade 1	00_H	AB-Step	AB_H	64-pin	XB_H	TLE989x	07_H
		AK-Step	BA_H	TLE98x1	$1X_H$		
				TLE98x3	$3X_H$		

Note: An 'X' within a hexadecimal value represents a "dont'care" position.

Figure 4 Customer ID decoding

3.3 Pin definitions

The functions and default states of the external pins are provided in **Table 3**.

The following pin types exist:

- I/O: Input or output
- I: Input only
- O: Output only
- P: Power supply

After reset, all pins have a defined setting. The following options are possible:

- Input with pull-up device enabled (I/PU)
- Input with pull-down device enabled (I/PD)
- Input with both pull-up and pull-down devices disabled (I/HiZ)
- Input floating to a voltage level (float)
- Input/Output with driver off (HiZ)
- Output with driver off and pull-down device enabled (PD)
- Output with driver off floating to a voltage level (float)
- Power supply (powered or GND)

Table 3 Pin definitions and functions

Symbol	**Pin no.**		**Type**	**Reset state**	**Function**	**Description**
	64	**48**				
General purpose I/Os						
P0.0	32	25	I/O	I/HiZ	GPIO	Connect to SWDCLK for debugging; Leave open if not used
P0.1	33	26	I/O	I/HiZ	GPIO	Leave open if not used
P0.2	34	27	I/O	I/HiZ	GPIO	Leave open if not used
P0.3	35	28	I/O	I/HiZ	GPIO	Leave open if not used
P0.4	36	–	I/O	I/HiZ	GPIO	Leave open if not used
P0.5	37	–	I/O	I/HiZ	GPIO	Leave open if not used
P0.6	38	–	I/O	I/HiZ	GPIO	Leave open if not used
P0.7	39	–	I/O	I/HiZ	GPIO	Leave open if not used
P0.8	40	–	I/O	I/HiZ	GPIO	Leave open if not used
P0.9	41	–	I/O	I/HiZ	GPIO	Leave open if not used
P0.10 or RESET	31	24	I/O	I/HiZ I/PU	GPIO or pin RESET	Configurable option (via 100TP); Leave open if not used
P1.0	25	20	I/O	I/HiZ	GPIO	Leave open if not used
P1.1	26	21	I/O	I/HiZ	GPIO	Leave open if not used
P1.2	27	22	I/O	I/HiZ	GPIO	Leave open if not used
P1.3	28	–	I/O	I/HiZ	GPIO	Leave open if not used
P1.4	29	–	I/O	I/HiZ	GPIO	Leave open if not used

Table 3 Pin definitions and functions (cont'd)

Symbol	Pin no.		Type	Reset state	Function	Description
	64	48				
Analog inputs						
P2.0	55	39	I	I/HiZ	GPI	Leave open if not used
P2.1	54	38	I	I/HiZ	GPI	Leave open if not used
P2.2	44	31	I	I/HiZ	GPI	Leave open if not used
P2.3	45	32	I	I/HiZ	GPI	Leave open if not used
P2.4	46	33	I	I/HiZ	GPI	Leave open if not used
P2.5	47	34	I	I/HiZ	GPI	Leave open if not used
P2.6	48	35	I	I/HiZ	GPI	Leave open if not used
P2.7	51	–	I	I/HiZ	GPI	Leave open if not used
P2.8	52	–	I	I/HiZ	GPI	Leave open if not used
P2.9	53	–	I	I/HiZ	GPI	Leave open if not used
CSAN	42	29	I	I/HiZ	CSA negative input	Connect via shunt resistor to CSAP; Connect to GNDVSSP if not used
CSAP	43	30	I	I/HiZ	CSA positive input	Connect via shunt resistor to CSAN; Connect to GNDVSSP if not used
Fail input/output						
FIFO	4	-	I/O	I/HiZ	Fail in /fail out	Connect via resistor to an external signal; Connect via 10 k pull-up to VDDP if not used
High-Voltage Monitoring inputs						
MON1	3	1	I	I/HiZ	HV monitor input 1	Connect via resistor to an external signal; Connect to GNDVSSP if not used
MON2	2	–	I	I/HiZ	HV monitor input 2	Connect via resistor to an external signal; Connect to GNDVSSP if not used
MON3	1	–	I	I/HiZ	HV monitor input 3	Connect via resistor to an external signal; Connect to GNDVSSP if not used
CAN interface						
CANH	64	48	I/O	HiZ	CAN high bus	Connect resistor to CANL; Leave open if not used
CANL	63	47	I/O	HiZ	CAN low bus	Connect resistor to CANH; Leave open if not used
VCAN	61	45	P	–	Supply input for CAN transceiver	Connect to VDDP; Connect capacitor to GNDCAN
GNDCAN	62	46	P	–	Ground for CAN transceiver	Connect to GNDVSSP; Connect capacitor to VCAN

Table 3 Pin definitions and functions (cont'd)

Symbol	Pin no.		Type	Reset state	Function	Description
	64	48				
Bridge Driver						
SL	22	19	I	GND	BDRV ground	Source low side FETs; Connect to GNDVSSP if not used
GL1	19	16	O	PD	BDRV gate low side 1	Connect to gate of low side MOSFET 1; Leave open if not used
GL2	20	17	O	PD	BDRV gate low side 2	Connect to gate of low side MOSFET 2; Leave open if not used
NC	21	18	–	–	–	2-phase device variant; Leave open
GL3	21	18	O	PD	BDRV gate low side 3	3-phase device variant; Connect to gate of low side MOSFET 3; Leave open if not used
SH1	13	10	I	Float to GND+1*Vdiode	BDRV source high 1	Connect to source of high side MOSFET 1; Leave open if not used
GH1	14	11	O	PD	BDRV gate high 1	Connect to gate of high side MOSFET 1; Leave open if not used
SH2	15	12	I	Float to GND+1*Vdiode	BDRV source high 2	Connect to source of high side MOSFET 2; Leave open if not used
GH2	16	13	O	PD	BDRV gate high 2	connect to gate of high side MOSFET 2; Leave open if not used
NC	17	14	–	–	–	2-phase device variant; Leave open
SH3	17	14	I	Float to GND+1*Vdiode	BDRV source high 3	3-phase device variant; Connect to source of high side MOSFET 3; Leave open if not used;
NC	18	15	–	–	–	2-phase device variant; Leave open
GH3	18	15	O	PD	BDRV gate high 3	3-phase device variant; Connect to gate of high side MOSFET 3; Leave open if not used;
Charge pump						
CP1L	8	5	O	HiZ	CP stage 1 out low	Connect external capacitor to CP1H; Leave open if not used
CP1H	9	6	O	Float to VSD-1*Vdiode	CP stage 1 out high	Connect external capacitor to CP1L; Leave open if not used
VCP	10	7	P	Float to VSD-1*Vdiode	charge pump output voltage	Connect via capacitor to star point of DC link high; Connect to VSD if not used
CP2L	12	9	O	HiZ	CP stage 2 out low	Connect external capacitor to CP2H; Leave open if not used

Table 3 Pin definitions and functions (cont'd)

Symbol	Pin no.		Type	Reset state	Function	Description
	64	48				
CP2H	11	8	O	Float to VSD-1*Vdiode	CP stage 2 out high	Connect external capacitor to CP2L; Leave open if not used
VSD	7	4	P	–	BDRV supply input	Connect with RC filter from star point of DC link high; Connect to VS if not used
VDH	6	3	I	I/HiZ	BRDV sense input	Connect with RC filter from star point of DC link high; Connect to SL if not used
Other pins						
TMS	30	23	I/O	I/PD	Test mode select input	Connect to SWDIO for debugging; Connect to GNDVSSP if not used
Power supply						
VS	5	2	P	–	Supply input	Connect via reverse polarity diode to VBAT; Connect capacitor to GNDVSSP
VDDP	24, 59	43	P	–	Output of VDDP regulator	Connect capacitor to GNDVSSP; Connect to VCAN
VDDC	56	40	P	–	Output of VDDC regulator	Connect capacitor to GNDVSSC
VDDEXT	60	44	P	–	Output of VDDEXT regulator	Connect capacitor to GNDVSSP; Connect to sensor supply input
GNDVSSP	23, 58	42	P	–	Ground of VDDP regulator	Connect capacitor to VDDP; Connect to module GND; Do not connect to GNDVSSC
GNDVSSC	57	41	P	–	Ground of VDDC regulator	Connect capacitor to VDDC; Do not connect to GNDVSSP
VAGND	49	36	P	–	Reference ground for mixed signal peripherals	If VREF5V is used: do not connect to GNDVSSP; If external reference is used: connect to GNDVSSP; Always connect via capacitor to VAREF
VAREF	50	37	P	–	Optional output of VREF5V regulator; Reference input for ADC1, SDADC, CSA, CSC	Connect to capacitor to VAGND; Optionally connect to VDDEXT or other reference; Leave open if not used
EP	–	–	P	–	Exposed pad	Connect to GNDVSSP

3.4 Special pin functions

3.4.1 RESET and FIFO pins

The following reset and fail-safe pins are available:

- RESET pin: P0.10 can be configured via a config sector setting (via 100TP) as bidirectional RESET function (default for P0.10 is GPIO)
- FIFO pin (only in 64 pin variant): this is a dedicated pin with bidirectional safe switch off (SSO) function

3.4.2 Programming

The device flash modules can be programmed using the following interfaces:

- Via standard Cortex SWD interface (pins TMS and P0.0, latched at start up, bootlatch) and SWD protocol
- Via bootstrap loader (BSL) interface (pins CANH and CANL) and UART protocol over CAN transceiver

Note: TMS is a dedicated pin. P0.0 is configured as SWDCLK in case TMS is latched high.

3.4.3 Debugging

The device can be debugged via standard Cortex SWD interface (pins TMS and P0.0) and SWD protocol.

Note: TMS is a dedicated pin. P0.0 is configured as SWDCLK in case TMS is latched high.

3.4.4 Clock input

- An external crystal or resonator can be connected to P2.0/XTALI and P2.1/XTALO
- An external digital clock can be connected to P2.0/XTALI

3.4.5 Analog reference

- The pins VAREF and VAGND serve as buffer for the analog reference voltage and analog reference ground for ADC1, CSA, CSC and SDADC
- A buffer capacitor (C_{VAREF}, P_ARVG_03_03) has to be placed externally

3.5 Device startup

After a device reset, the BootROM firmware is executed to initialize the device.

The execution of the BootROM firmware has a certain execution time until execution is handed over to the user application.

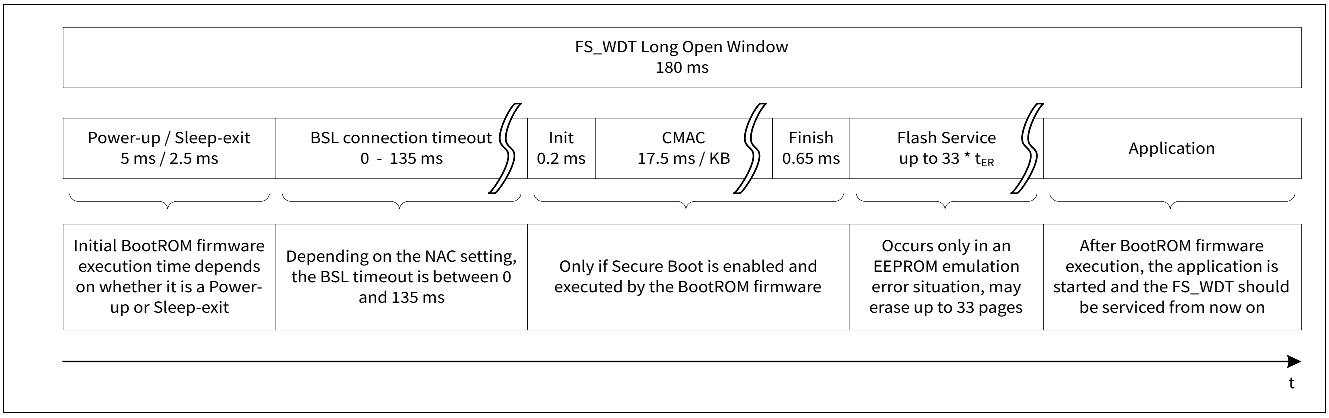


Figure 5 Device bootup timing

Note: The Power-up, Sleep-exit, and FS_WDT Long Open Window timings refer to typical values of MCLK. The timings for the BSL connection timeout and Secure Boot refer to typical values of HP_CLK.

3.6 Brown-out

The integrated VDDP regulator will enter dropout operation as the VS pin voltage is dropping below the minimum supply voltage (P_GEN_09_01). As a consequence the regulator will enter dropout and can no longer maintain its output voltage within the regulation limits.

The MCU subsystem remains fully functional down to the minimum extended supply voltage range (P_GEN_09_03 and P_GEN_09_14).

Care should be taken while operating following peripherals under low-supply conditions:

- Derated electrical performance for VDDEXT, VREF5V (VAREF), CSA, CSC, SDADC, MON, BDRV
- Derated ADC1 electrical performance (relating to a drift on the VREF5V (VAREF) reference)
- CAN transceiver interface

Figure 6 illustrates the operation under low-supply (brown-out) conditions:

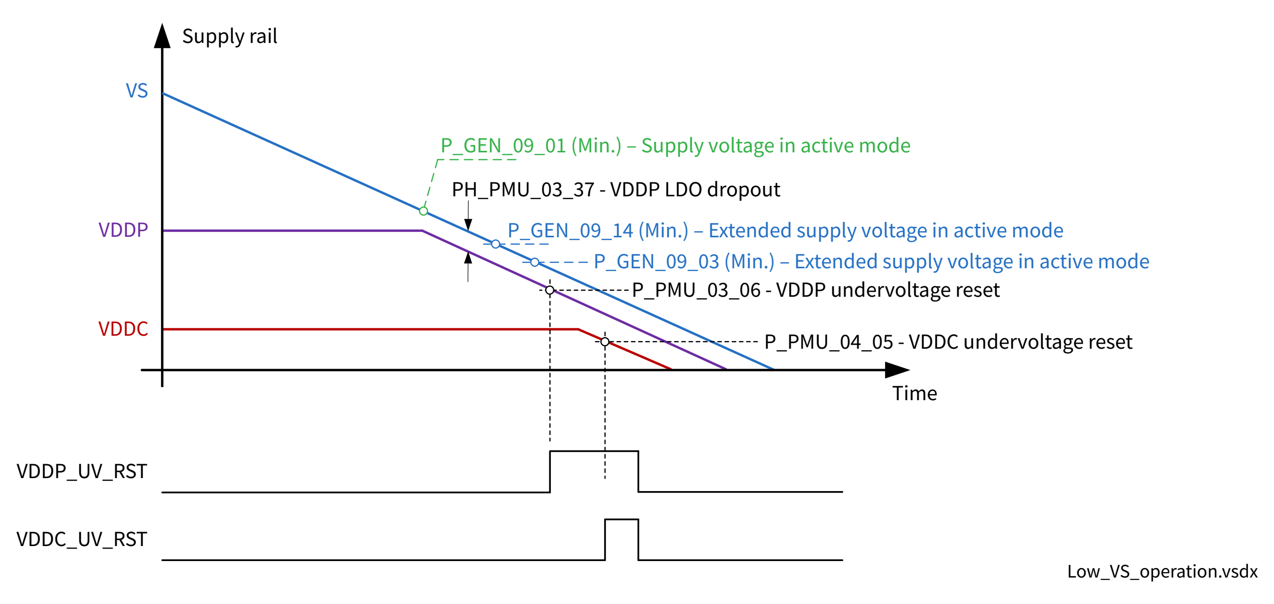


Figure 6 Operation under low-supply (brown-out) conditions

3.7 General electrical characteristics

3.7.1 Absolute maximum ratings

Table 4 Voltages Supply Pins

Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VS voltage	V_{S_max}	-0.3	-	40	V	[1] Load dump; *t*=400ms	P_GEN_01_01
VSD voltage max1	V_{SD_max1}	-0.3	-	48	V	[1]	P_GEN_01_02
VSD voltage max2	V_{SD_max2}	-2.8	-	48	V	[1] For -2.8V external 2.2Ω is required to limit the output current; t=8ms	P_GEN_01_03
VDDP voltage	V_{DDP_max}	-0.3	-	5.5	V	[1]	P_GEN_01_04
VDDEXT voltage	V_{DDEXT_max}	-0.3	-	V_S+0.3	V	[1]	P_GEN_01_05
VCAN voltage	V_{CAN_max}	-0.3	-	5.5	V	[1]	P_GEN_01_06
VDDC voltage	V_{DDC_max}	-0.3	-	1.6	V	[1]	P_GEN_01_07
Analog reference voltage	V_{AREF_max}	-0.3	-	VDDP +0.3	V	[1] VAREF < VDDP_max; between pin VAREF and VAGND	P_GEN_01_08
Analog reference ground	V_{AGND_max}	-0.3	-	0.3	V	[1]	P_GEN_01_09

1) Not subject to production test, specified by design

Table 5 Voltages High Voltage Pins

Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage at MONx pins	V_{MON_max}	-28	-	40	V	[1] The overload current must be limited via an external 1kΩ resistor at pin	P_GEN_02_01
Voltage at VDH pin	V_{VDH_max}	-2.8	-	48	V	[1] The overload current must be limited via an external 1kΩ resistor at pin	P_GEN_02_02
Voltage at GHx pins	V_{GH}	-8	-	48	V	[1]	P_GEN_02_03

Table 5 Voltages High Voltage Pins (cont'd)

Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage at GHx vs. SHx pins	V_{GHvsSH}	-0.3	-	14	V	[1]	P_GEN_02_04
Voltage at SHx pins	V_{SH}	-8	-	48	V	[1]	P_GEN_02_05
Voltage at GLx pins	V_{GL}	-8	-	48	V	[1]	P_GEN_02_06
Voltage at GLx vs. SL pins	V_{GLvsSL}	-0.3	-	14	V	[1]	P_GEN_02_07
Voltage at SL pin	V_{SL}	-8	-	48	V	[1]	P_GEN_02_08
Voltage at charge pump pins CP1H, CP1L, CP2H, CP2L, VCP	V_{CPx}	-0.3	-	48	V	[1] Limit output current to I_{CPx} > -200µA	P_GEN_02_09
Voltage at FIFO pin	V_{FIFO_max}	-28	-	40	V	[1] The overload current must be limited via an external 1 kΩ resistor at pin	P_GEN_02_10

1) Not subject to production test, specified by design

Table 6 Voltages CAN Transceiver

Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage on CANH, CANL	V_{Bus_max}	-27	-	40	V	[1]	P_GEN_03_01
Differential voltage	V_{diff}	-5	-	10	V	[1] $V_{diff} = V_{CANH} - V_{CANL}$	P_GEN_03_02

1) Not subject to production test, specified by design

Table 7 Voltages GPIOs

Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage on port pin P0.x, P1.x, P2.x, TMS	V_{IN}	-0.3	-	V_{DDP}+0.3	V	[1] $V_{IN}<V_{DDP\_max}$	P_GEN_04_01

1) Not subject to production test, specified by design

Table 8 Voltages at Current Sense Amplifier Inputs

Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage CSAN, CSAP	V_{OAI}	-7	-	7	V	[1]	P_GEN_05_01

[1] Not subject to production test, specified by design

Table 9 Currents

Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Max. current at VCP pin	I_{VCP}	-15	-	-	mA	[1]	P_GEN_06_02

[1] Not subject to production test, specified by design

Table 10 Overload currents

Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overload current on digital inputs P0.x, P1.x, TMS	I_{ovdig}	-2	-	2	mA	[1] [2] [3] Overload current must be limited, e.g. via series resistor	P_GEN_06_01
Overload current on analog inputs P2.x (except P2.0, P2.1 and P2.5)	I_{ovana}	-1	-	2	mA	[1] [2] [3] Overload current must be limited, e.g. via series resistor	P_GEN_06_04
Sum of overload currents	I_{ovsum}	-4	-	4	mA	[1] [2] [3] The number of pins with overload must be limited to maximum 4 pins	P_GEN_06_03

[1] Overload current is allowed in following operation modes: unpowered, active and sleep mode

[2] Overload conditions occur if the standard operating conditions are exceeded, i.e. the input voltage V_{IN} at the pin exceeds the specified range: $V_{IN} > VDDP + 0.3$ V (Iov > 0) or $V_{IN} < -0.3$ V (Iov < 0)

[3] Not subject to production test, specified by design

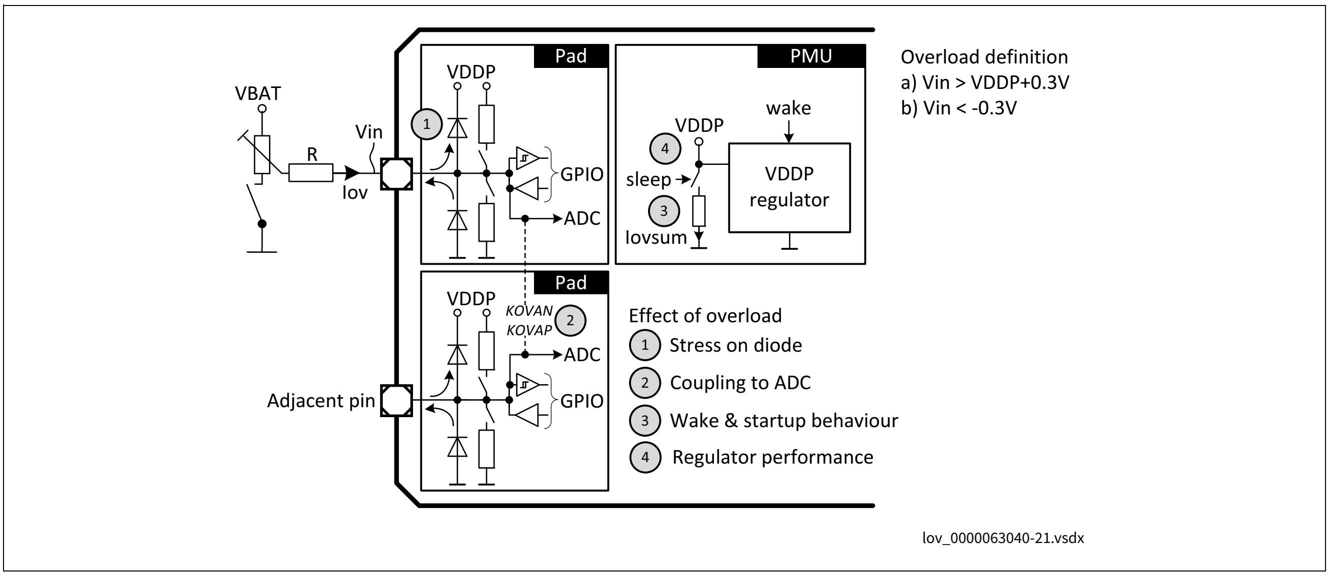


Figure 7 Overload current

Table 11 Temperatures

Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction temperature	T_j	-40	-	175	°C	[1]	P_GEN_07_01
Storage temperature	T_{stg}	-55	-	175	°C	[1]	P_GEN_07_02

[1] Not subject to production test, specified by design

EMC

EMC susceptibility according to BISS generic IC test specification, release 2.0.

Table 12 ESD susceptibility

Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ESD susceptibility **HBM** all pins	V_{ESD1}	-2	-	2	kV	[1] [2]	P_GEN_08_01
ESD susceptibility **CDM**	V_{ESD_CDM}	-500	-	500	V	[2] Charged device model, acc. JEDEC JESD22-C101	P_GEN_08_08
ESD susceptibility **CDM** on corner pins	$V_{ESD\_CDM\_Corner}$	-750	-	750	V	[2] Charged device model, acc. JEDEC JESD22-C101	P_GEN_08_09

1) ESD susceptibility, "JEDEC HBM" according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)
2) Not subject to production test, specified by design

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.7.2 Functional range

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

Table 13 Functional Range

Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage at VS in active mode - voltage range 1	V_{S_act1}	5.5	-	28	V		P_GEN_09_01
Extended supply voltage at VS in active mode - voltage range 2	V_{S_act2}	28	-	40	V	Allowed for t_{max} < 400ms with parameter deviation	P_GEN_09_02
Extended supply voltage at VS in active mode - voltage range 3	V_{S_act3}	3.0	-	5.5	V	Due to derived voltage dependency following modules show parameter deviation: VDDEXT, VREF5V, CSA, CSC, SDADC, MON, BDRV. Module CANTRX is out of its functional range	P_GEN_09_03
Extended supply voltage at VS in active mode - voltage range 4	V_{S_act4}	4.2	-	5.5	V	[1] Due to dependency to VAREF, the ADC1 shows parameter deviations	P_GEN_09_14
Supply voltage at VS in sleep mode	V_{S_slpmin}	3.0	-	-	V		P_GEN_09_07
Supply voltage at VS in stop mode	V_{S_stpmin}	3.0	-	-	V		P_GEN_09_06
Supply voltage transients slew rate	$\Delta V_S/\Delta t$	-5	-	5	V/µs	[2] For rising and falling transient: not faster than this	P_GEN_09_08
Supply voltage at VSD in active mode for bridge driver supply	V_{SD_act1}	5.4	-	29	V		P_GEN_09_04

Table 13 Functional Range (cont'd)

Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Extended maximum supply voltage at VSD in active mode for bridge driver supply	V_{SD_act2}	29	-	32	V	Allowed for t_{max} < 400ms with parameter deviation	P_GEN_09_05
Extended supply voltage at VSD in active mode for bridge driver supply - active brake	V_{SD_ab}	29	-	40	V	Active brake mode with low-side drivers, charge pump off	P_GEN_09_16
Analog reference voltage	V_{AREF}	3.8	-	VDDP +0.3	V	[2] between pin VAREF and VAGND	P_GEN_09_15
Analog reference voltage ground	V_{AGND}	-0.05	-	0.05	V	[2] at VAGND pin	P_GEN_09_17
Output sum current for all GPIO pins	$I_{GPIO,sum}$	-50	-	50	mA	[3] [2]	P_GEN_09_11
System frequency 0	f_{sys0}	5	-	60	MHz		P_GEN_09_12
System frequency 1	f_{sys1}	5	-	80	MHz		P_GEN_09_13

1) ADC1 calibration is done at VS = 13.5 V and VAREF = 5.0 V, for low VS range calibration shall be disabled (CALEN.CALENi = 0) and VAREF measurement from ADC2 shall be used

2) Not subject to production test, specified by design

3) This is a system requirement; it has to be ensured that current stays within limits

3.7.3 Current consumption

Table 14 Current Consumption

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption in active mode	I_{Vs_act60}	-	-	60	mA	V_S=3V to 28V; see **Table 15 Active mode current consumption**	P_GEN_10_01
Current consumption in active mode with reduced frequency	I_{Vs_act20}	-	-	50	mA	V_S=3V to 28V; see **Table 15 Active mode current consumption**	P_GEN_10_02
Current consumption in active mode at reduced frequency and with CAN communication only	I_{Vs_actCAN}	-	-	35	mA	V_S=3V to 28V; see **Table 15 Active mode current consumption**	P_GEN_10_03
Current consumption in sleep mode at normal voltage and temperature range	I_{Vs_slp0}	-	-	35	µA	V_S=9V to 28V; T_J=-40°C to 85°C; see **Table 16 Sleep mode current consumption**	P_GEN_10_04
Current consumption in sleep mode at low voltage and normal temperature range	I_{Vs_slp1}	-	-	50	µA	V_S=5.5V to 9V; T_J=-40°C to 85°C; see **Table 16 Sleep mode current consumption**	P_GEN_10_05
Current consumption in sleep mode at extended voltage range and temperature range	I_{Vs_slp2}	-	-	250	µA	V_S=3V to 28V; T_J=-40°C to 150°C; see **Table 16 Sleep mode current consumption**	P_GEN_10_06
Current consumption in stop mode - temperature range 1	I_{Vs_stp1}	-	-	120	µA	T_J=-40°C to 25°C; see **Table 17 Stop mode current consumption**	P_GEN_10_11
Current consumption in stop mode - temperature range 2	I_{Vs_stp2}	-	-	175	µA	T_J=25°C to 85°C; see **Table 17 Stop mode current consumption**	P_GEN_10_12

Table 14 Current Consumption (cont'd)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption in stop mode - temperature range 3	I_{Vs_stp3}	-	-	2.2	mA	T_J=85°C to 175°C; see **Table 17 Stop mode current consumption**	P_GEN_10_13
Current consumption in stop mode - extended voltage range	I_{Vs_stp4}	-	-	6	mA	V_S=3V to 28V; T_J=-40°C to 175°C; see **Table 17 Stop mode current consumption**	P_GEN_10_14
Current consumption of one MONx as wake source in sleep or stop mode	I_{Vs_MONx}	-	-	1	µA	[1] Additional to Ivs_slp, Ivs_stp if configured	P_GEN_10_23
Current consumption of CAN as wake source in sleep or stop mode	I_{Vs_CAN}	-	-	4	µA	[1] Additional to Ivs_slp, Ivs_stp if configured	P_GEN_10_24
Current consumption of CYCLIC TIMER as wake source in sleep or stop mode	I_{Vs_CYC}	-	-	5	µA	[1] Additional to Ivs_slp, Ivs_stp if configured; while VDDEXT is off	P_GEN_10_25
Current consumption of one GPIO as wake source in stop mode	I_{Vs_GPIO}	-	-	1	µA	[1] Additional to Ivs_slp, Ivs_stp if configured	P_GEN_10_26
Current consumption at pin VSD - bridge driver fully operating	I_{VSD_on}	-	-	70	mA	3x HS/LS @ 20 kHz with 6x C_L=10nF; 5.4V≤V_{SD}≤29V	P_GEN_10_18

Table 14 Current Consumption (cont'd)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption at pin VSD - bridge driver in active brake mode	I_{VSD_ab}	-	-	10	mA	3x LS statically on; $5.4V \le V_{SD} \le 40V$	P_GEN_10_19
Current consumption at pin VSD - bridge driver off	I_{VSD_off}	-	-	5	µA	3x HS and LS off with passive pulldown	P_GEN_10_22

1) Not subject to production test, specified by design

Table 15 Active mode current consumption

	I_{Vs_act60}	I_{Vs_act20}	I_{Vs_actCAN}
PLL0/PLL1	locked on XTAL	locked on XTAL	locked on XTAL
SYS0_CLK (for MCU)	60 MHz	20 MHz	20 MHz
SYS1_CLK (for CAN)	80 MHz	80 MHz	80 MHz
MCU subsystem	active	active	active with CPU DEEPSLEEP mode
Timers, UARTs, SSCs	active	active	disabled
ADC1, CSA/CSC	converting	converting	disabled
CANTRX, MultiCAN	receiving, 2 Mbit	receiving, 2 Mbit	receiving, 2 Mbit
BDRV, CP	PWM @3ph with 20 KHz	PWM @3ph with 20 KHz	disabled
VDDEXT	disabled	disabled	disabled
GPIO	input without load	input without load	input without load
Wake configuration	via MON1	via MON1	via MON1

Table 16 Sleep mode current consumption

	I_{Vs_slp0}	I_{Vs_slp1}	I_{Vs_slp2}	I_{Vs_slp3}
PLL0/PLL1	OFF	OFF	OFF	OFF
SYS0_CLK (for MCU)	OFF	OFF	OFF	OFF
SYS1_CLK (for CAN)	OFF	OFF	OFF	OFF
MCU subsystem	OFF	OFF	OFF	OFF
Timers, UARTs, SSCs	OFF	OFF	OFF	OFF
ADC1, CSA/CSC	OFF	OFF	OFF	OFF
CANTRX, MultiCAN	OFF	OFF	OFF	OFF

Table 16 Sleep mode current consumption

	$I_{\mathrm{Vs\_slp0}}$	$I_{\mathrm{Vs\_slp1}}$	$I_{\mathrm{Vs\_slp2}}$	$I_{\mathrm{Vs\_slp3}}$
BDRV, CP	SSO active	SSO active	SSO active	SSO active
VDDEXT	OFF	OFF	OFF	OFF
GPIO	no load	no load	no load	no load
Wake configuration	via MON1	via MON1	via MON1	via MON1

Table 17 Stop mode current consumption

	$I_{\mathrm{Vs\_stp1}}$	$I_{\mathrm{Vs\_stp2}}$	$I_{\mathrm{Vs\_stp3}}$	$I_{\mathrm{Vs\_stp4}}$
PLL0/PLL1	OFF	OFF	OFF	OFF
SYS0_CLK (for MCU)	OFF	OFF	OFF	OFF
SYS1_CLK (for CAN)	OFF	OFF	OFF	OFF
MCU subsystem	stopped	stopped	stopped	stopped
Timers, UARTs, SSCs	OFF	OFF	OFF	OFF
ADC1, CSA/CSC	OFF	OFF	OFF	OFF
CANTRX, MulitCAN	OFF	OFF	OFF	OFF
BDRV, CP	SSO active	SSO active	SSO active	SSO active
VDDEXT	OFF	OFF	OFF	OFF
GPIO	no load	no load	no load	no load
Wake configuration	via MON1	via MON1	via MON1	via MON1

3.7.4 Thermal resistance

Table 18 Thermal Resistance - TQFP-48

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case for TQFP-48	$R_{\mathrm{thjc\_T48}}$	-	6	-	K/W	1)	P_GEN_12_01
Junction to ambient for TQFP-48	$R_{\mathrm{thja\_T48}}$	-	33	-	K/W	2) 1)	P_GEN_12_02

1) Not subject to production test, specified by design

2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board. Board: 76.2x114.3x1.5mm^3 with 2 inner copper layers (35µm thick), with thermal via array under the exposed pad contacting the first inner copper layer and 300mm^2 cooling area on the bottom layer (70µm).

Table 19 Thermal Resistance - LQFP-64

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case for LQFP-64	$R_{\mathrm{thjc\_L64}}$	-	6	-	K/W	1)	P_GEN_13_01
Junction to ambient for LQFP-64	$R_{\mathrm{thja\_L64}}$	-	33	-	K/W	2) 1)	P_GEN_13_02

1) Not subject to production test, specified by design

2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board. Board: 76.2x114.3x1.5mm^3 with 2 inner copper layers (35µm thick), with thermal via array under the exposed pad contacting the first inner copper layer and 300mm^2 cooling area on the bottom layer (70µm).

3.7.5 Timing characteristics

Table 20 System Timing

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power-up time	$t_{startup}$	-	-	5	ms	[1] VS ramp-up (0 V to 14 V in 100 µs) until start of user code	P_GEN_14_01
Sleep-Exit	t_{slpex}	-	-	2.5	ms	[1] CAN/MON wake event until start of user code	P_GEN_14_02
Sleep-Entry	t_{slpen}	-	-	0.2	ms	[1] From setting PMCON0.SLEEP	P_GEN_14_03
Stop-Exit	t_{stpex}	-	-	0.3	ms	[1] CAN/MON/GPIO wake event until start of user code	P_GEN_14_04
Stop-Entry	t_{stpen}	-	-	0.2	ms	[1] From setting PMCON0.STOP	P_GEN_14_06

1) Not subject to production test, specified by design

4 BLDC driver application information

Figure 8 shows the TLE989x/TLE988x in an electric drive application setup controlling a BLDC motor.

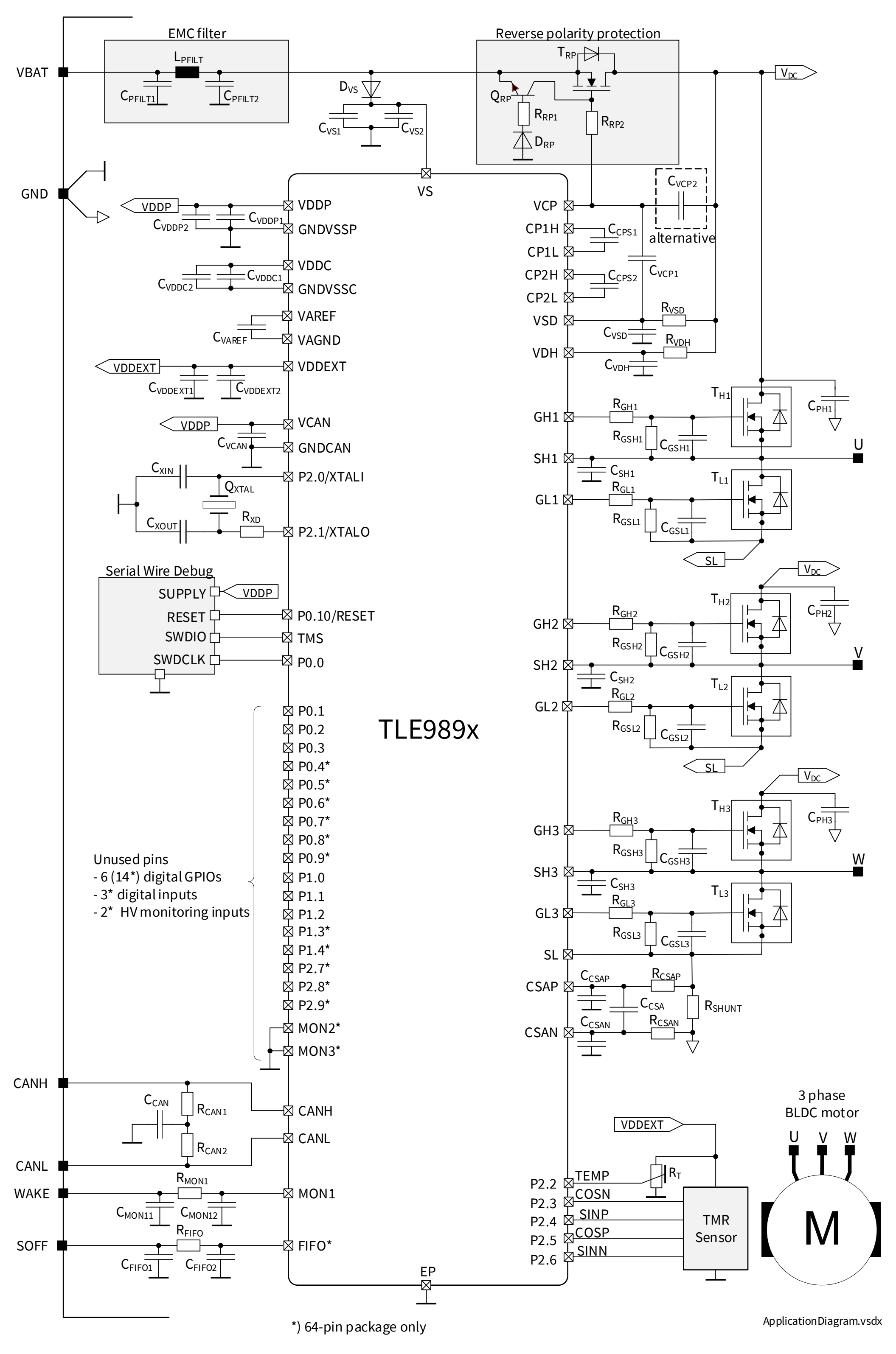


Figure 8 Simplified application diagram example for a BLDC system

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. This is a very simplified example of an application circuit and bill of material. The function must be verified in the actual application.

Table 21 External components (BOM)

Symbol	Function	Component
D_{VS}	Reverse polarity protection diode	e.g. BAS52-02V
C_{VS1}	Decoupling capacitor at VS pin	see P_PMU_01_06
C_{VS2}	Buffer capacitor at VS pin	see P_PMU_01_07
C_{VDDP1}	Decoupling capacitor at VDDP pin	see P_PMU_03_22
C_{VDDP2}	Stability capacitor at VDDP pin	see P_PMU_03_22
$C_{VDDEXT1}$	Decoupling capacitor at VDDEXT pin	see P_PMU_05_13
$C_{VDDEXT2}$	Stability capacitor at VDDEXT pin	see P_PMU_05_13
C_{VCAN}	Decoupling capacitor at VCAN pin	see P_PMU_03_23
C_{VDDC1}	Decoupling capacitor at VDDC pin	see P_PMU_04_21
C_{VDDC2}	Decoupling capacitor at VDDC pin	see P_PMU_04_21
C_{VAREF}	Stability capacitor at VAREF pin	see P_ARVG_03_03
C_{CPS1}	Charge pump flying capacitor stage 1	application dependent, min. 100 nF
C_{CP2S}	Charge pump flying capacitor stage 2	application dependent, min. 100 nF
C_{VCP1}	Charge pump storage capacitor (placing option 1)	application dependent, min. 220 nF
C_{VCP2}	Charge pump storage capacitor (placing option 2)	application dependent, min. 220 nF
R_{MON1}	Resistor at MON1 pin for ISO pulses	application dependent, e. g. 1 kΩ
C_{MON11}	Pi Filter Capacitor at MONx	application dependent, e. g. 10 nF
C_{MON12}	Pi Filter Capacitor at MONx	application dependent, e. g. 1 nF
R_{FIFO}	Resistor at FIFO pin for ISO pulses	application dependent, e. g. 1 kΩ
C_{FIFO1}	Pi Filter Capacitor at FIFO pin	application dependent, e. g. 10 nF
C_{FIFO2}	Pi Filter Capacitor at FIFO pin	application dependent, e. g. 1 nF
C_{PH1}	DC link capacitor	application dependent, e. g. 680 µF
C_{PH2}	DC link capacitor	application dependent, e. g. 680 µF
C_{PH3}	DC link capacitor	application dependent, e. g. 680 µF
C_{CSA}	Filter capacitor	application dependent, e. g. 1 nF
R_{CSAN}	Filter resistor (optional)	application dependent, e. g. 12 Ω
R_{CSAP}	Filter resistor (optional)	application dependent, e. g. 12 Ω
C_{CSAN}	Filter capacitor (optional)	application dependent, e. g. 1 nF
C_{CSAP}	Filter capacitor (optional)	application dependent, e. g. 1 nF
R_{SHUNT}	Shunt resistor	application dependent, e. g. 5 mΩ
R_{VSD}	Limitation of reverse current due to transient (-2 V, 8 ms)	2 Ω

Table 21 External components (BOM) (cont'd)

Symbol	Function	Component
C_{VSD}	Capacitor	1 µF
R_{VDH}	Filter resistor	optional, e. g. 1 kΩ
C_{VDH}	Filter capacitor	optional, e. g. 100 nF
$R_{GH1/2/3}$	Resistor	optional, 2 Ω
$R_{GL1/2/3}$	Resistor	optional, 2 Ω
$R_{GSH1/2/3}$	Resistor	optional, 100 kΩ
$R_{GSL1/2/3}$	Resistor	optional, 100 kΩ
$C_{GSH1/2/3}$	Capacitor	optional, 4.7 nF
$C_{GSL1/2/3}$	Capacitor	optional, 4.7 nF
$T_{H1/2/3}$	N-channel MOSFET	e.g. IPC70N04S5-4R6
$T_{L1/2/3}$	N-channel MOSFET	e.g. IPC70N04S5-4R6
T_{RP}	Reverse polarity protection MOSFET	e.g. IPC70N04S5-4R6
Q_{RP}	Reverse polarity protection transistor	e.g. BC817
R_{RP1}	Reverse polarity protection resistor 1	10 kΩ
R_{RP2}	Reverse polarity protection resistor 2	3.3 kΩ
D_{RP}	Reverse polarity protection circuit diode	e.g. BAS52-02V
L_{PFILT}	EMC filter coil	e.g. 4.7 µH
$C_{PFILT1/2}$	EMC filter capacitor	e.g. 22 µF
$C_{SH1/2/3}$	Capacitor	optional
R_{SH2}	Resistor	optional
R_{SH3}	Resistor	optional
Q_{XTAL}	Crystal or ceramic resonator	optional , e. g. NG3225GA, 16 MHz
R_{XD}	Damping resistor	optional, e. g. 330 Ω
C_{XIN}	Capacitor	optional, e. g. 0 Ω
C_{XOUT}	Capacitor	optional, e. g. 4.7 pF
C_{CAN}	Capacitor	optional, e. g. 4.7 nF
$R_{CAN1/2}$	Resistor	optional, e. g. 62 Ω
R_T	Thermal resistor (e. g. NTC)	optional
TMR	TMR sensor	optional, e. g. TLE5501

4.1 Further application information

- Please contact Infineon Technologies for information regarding the pins FMEA and Safety Manual
- For further information, please follow the link: **https://www.infineon.com/motixmcu**

5 Power Management Unit (PMU)

5.1 Features overview

The Power Management Unit (PMU) manages all functions related to the device power supply and its supervision. The PMU controls all operating mode transitions and ensures a fail-safe behavior.

The PMU provides following features:

- State control
  - Operating state machine (Start-up, Active, Stop, Sleep and Fail-Sleep)
  - Voltage regulator control
  - Master clock generation (MCLK) acting as PMU clock
  - Reset management controlling the reset behavior of the entire device
  - Bi-directional reset pin (P0.10/RESET) as reset input and reset output indicating an internally generated reset
  - Wake-up control for wake-up in Stop/Sleep modes via MON, CAN, BDRV, GPIOs, cyclic timer
- Voltage regulators
  - Linear voltage regulators (VMSUP) for internal supply of the device
  - Linear voltage regulator (VDDP, 5 V typ.) for GPIO and CAN transceiver supply
  - Linear voltage regulator (VDDC, 1.5 V typ.) for internal digital logic supply
  - Reference voltage generation (VAREFSUP)
  - Linear voltage regulator (VDDEXT, 5 V typ.) for external sensors supply
- Fail-safe supervision
  - System monitor, monitoring of fail-safe relevant signals
  - Supply monitor, monitoring of fail-safe relevant voltages
  - Safe reference clock (REF_CLK) and clock watchdog for monitoring of the MCLK
  - Fail-safe input/output (FIFO pin) for external safe shutdown request or indication
  - Fail-safe window watchdog (FS_WDT) for monitoring the CPU execution timing
  - Safe shutdown mechanism to bring the bridge driver (BDRV) into a safe off-state
- Retention memory (GPUDATA with 96 bits) for data storage in Sleep and Fail-sleep modes

5.2 Block diagram

The PMU module consists of the following major functional parts:

- State control
- Voltage regulators
- Fail-safe supervision
- Retention memory

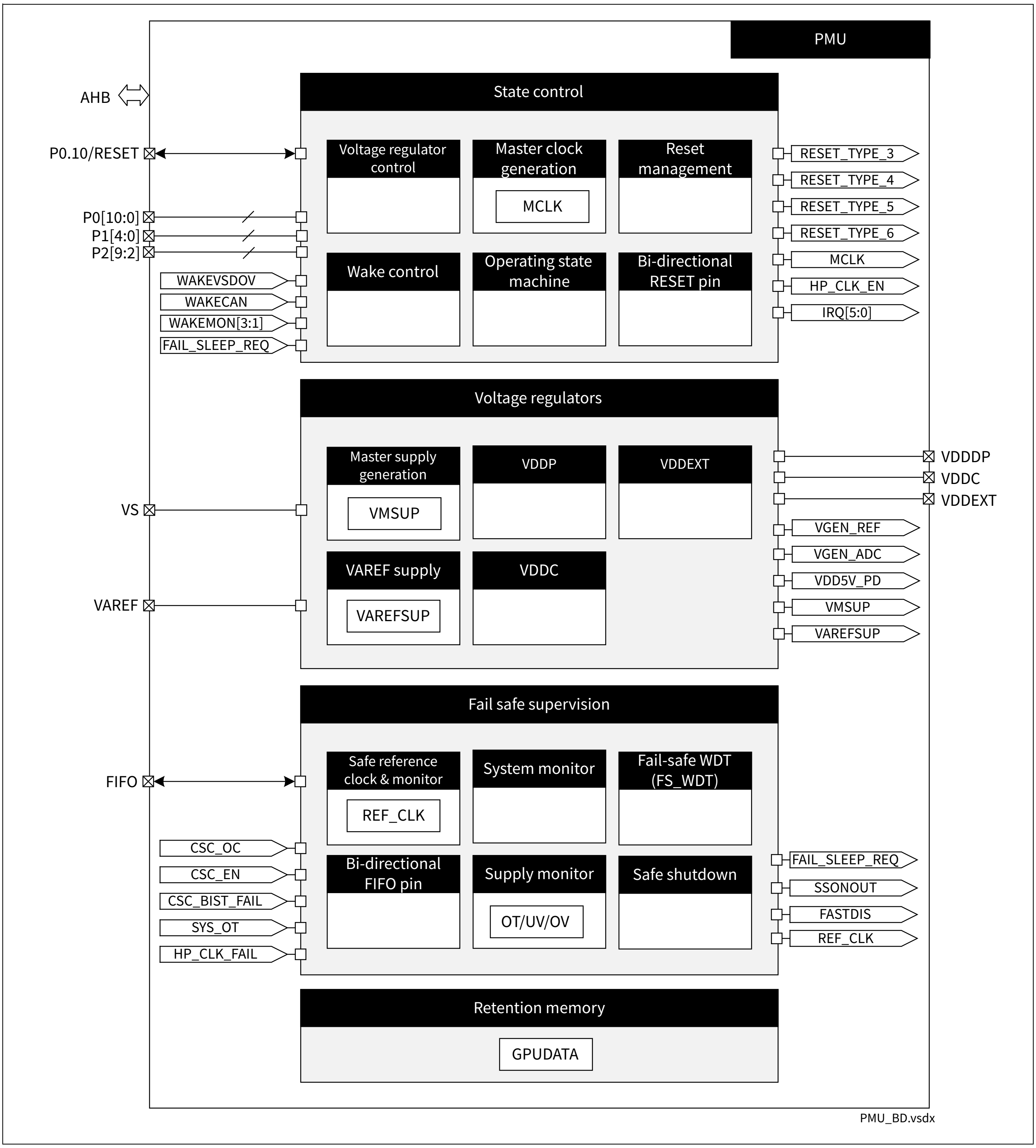


Figure 9 Block diagram PMU

5.3 Electrical characteristics PMU

5.3.1 Supply characteristics

Table 22 PMU Supply DC Specification

Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
External Supply in regulation mode	V_S	5.5	13.5	28	V	[1]	P_PMU_01_01
VS input voltage transient time	t_{VSSLEW}	5	-	-	µs	[1] V_S voltage rise time rate from 0V to 28V	P_PMU_01_05
Required V_S input capacitance	C_{VS1}	0.1	-	-	µF	[1] Buffering capacitor to cut off battery spikes, value depending on application requirements, ESR < 1Ω;	P_PMU_01_06
Required V_S input capacitance	C_{VS2}	10	-	-	µF	[1]	P_PMU_01_07

1) Not subject to production test, specified by design

5.3.2 Voltage regulators

5.3.2.1 Master supply characteristics

Table 23 Master Supply DC Specification

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Master Supply output voltage	V_{MSUP}	1.4	1.5	1.6	V	all parameters within specification limits	P_PMU_02_01
Master Supply overvoltage threshold	V_{MSUPOV}	1.65	1.72	1.79	V		P_PMU_02_02
Master Supply overvoltage filter time (analog)	$t_{VMSUPOVFT}$	1	-	3	µs	[1] Step on VMSUP from VMSUP@typ to VMSUPOV@max	P_PMU_02_03

Table 23 Master Supply DC Specification (cont'd)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Master Supply input voltage in regulation mode	V_{MSUPIN}	5.5	12	28	V	[1]	P_PMU_02_04
Master Supply undervoltage threshold	V_{MSUPUV}	1.2	1.275	1.35	V		P_PMU_02_06
Master Supply undervoltage filter time (analog)	$t_{MSUPUVFT}$	1	-	3	µs	[1] Step on VMSUP from VMSUP@typ to VMSUPUV@min	P_PMU_02_07
Central PMU bandgap reference voltage measured at ADC2	V_{GEN_ADC}	1.0	1.1	1.3	V		PH_PMU_02_18

1) Not subject to production test, specified by design

5.3.2.2 VDDP characteristics

Table 24 VDDP DC Specification

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VDDP output voltage including line and load regulation	V_{DDP}	4.9	5.0	5.1	V	all parameters within specification limits 1mA ≤ IDDP ≤ 170mA; VDDP regulator in high current mode	P_PMU_03_01
VDDP output current @ High Current Mode (HCM)	I_{DDPHCM}	0	-	170	mA	[1] external 5V Supply, Supply for VDDC regulator	P_PMU_03_03
VDDP output current @ Low Current Mode (LCMN and LCMA)	$I_{DDPLCM1}$	0	-	2	mA	[1] external 5V Supply, Supply for VDDC regulator	P_PMU_03_04
VDDP output current @ Low Current Mode (LCMN and LCMA)	$I_{DDPLCM2}$	0	-	7	mA	[1] external 5V Supply, Supply for VDDC regulator	P_PMU_03_05

Table 24 VDDP DC Specification (cont'd)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VDDP undervoltage falling threshold	$V_{DDPUVFALL}$	2.55	2.67	2.77	V		P_PMU_03_06
VDDP undervoltage rising threshold	$V_{DDPUVRISE}$	2.65	2.77	2.87	V	[1]	P_PMU_03_07
VDDP undervoltage filter time	$t_{VDDPUVFT}$	0.85	1	1.15	µs	[1]	P_PMU_03_09
VDDP undervoltage warning falling threshold	$V_{DDPUVWFALL}$	4.34	4.52	4.7	V		P_PMU_03_10
VDDP undervoltage warning rising threshold	$V_{DDPUVWRISE}$	4.44	4.62	4.8	V	[1]	P_PMU_03_11
VDDP undervoltage warning filter time	$t_{VDDPUVWFT}$	1	2	3	µs	[1]	P_PMU_03_12
VDDP overvoltage falling threshold	$V_{DDPOVFALL}$	5.554	5.785	6.016	V	[1]	P_PMU_03_13
VDDP overvoltage rising threshold	$V_{DDPOVRISE}$	5.666	5.902	6.138	V		P_PMU_03_14
VDDP current limitation	$I_{DDPILIM}$	500	700	900	mA	current flowing out of the pin, V_{DDP} = 0V	P_PMU_03_16
VDDP current limitation filter time	$t_{VDDPILIMFT}$	2	4	6	µs	[1]	P_PMU_03_17
VDDP overtemperature threshold	$T_{jVDDPOTSHD}$	180	190	200	°C	[1]	P_PMU_03_18
VDDP ripple rejection	$PSRR_{VDDP}$	40	-	-	dB	[1] @10 ... 20 KHz; @0.5Vpp; 6V ≤ V_S ≤ 28V; I_{DDPHCM} = 85mA; VDDP regulator in high current mode	P_PMU_03_20
Required VDDP output buffer capacitance	C_{VDDP}	0.57	-	4.4	µF	[1] ESR < 0.1Ω; the specified capacitor value is a value including tolerances	P_PMU_03_22

Table 24 VDDP DC Specification (cont'd)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Buffer Capacitance on CAN transceiver supply to counter EMI	C_{VCAN}	1	-	3.83	µF	[1] Total capacitance of C_{VDDP1}, C_{VDDP2} and C_{VCAN} shall not exceed 4.4µF in order to ensure startup time within specification. The specified capacitor value is a value including tolerances	P_PMU_03_23
VDDP_REG current consumption@LCM 1, adaptive on or off	$I_{VDDPREGLCM1}$	-	-	29	µA	[1] Low-Current Mode 1; IDDPLCM1 ≤ 60 µA; -40°C<T_J<85°C	PH_PMU_03_24
VDDP_REG current consumption@LCM 2, adaptive on or off	$I_{VDDPREGLCM2}$	-	-	39	µA	[1] Low-Current Mode 2; IDDPLCM1 ≤ 60 µA; -40°C<T_J<85°C	PH_PMU_03_42
VDDP output voltage@short circuit on CAN, High Current Mode (HCM)	$V_{DDPSHORT}$	4.75	5.0	5.25	V	170mA<I_{DDP}≤240mA	PH_PMU_03_30
VDDP output voltage including line and load regulation@Low Current Mode (LCM)	$V_{DDPLCMN}$	4.9	-	5.15	V	1µA≤I_{DDP}≤$I_{DDPLCM1/2@max}$	PH_PMU_03_32
VDDP output drop	$V_{DDPDROP}$	0	-	450	mV	I_{DDP}=125mA; V_S=3.0V	PH_PMU_03_37

1) Not subject to production test, specified by design

5.3.2.3 VDDC characteristics

Table 25 VDDC DC Specification

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VDDC output voltage including line and load regulation in HCM and LCM	V_{DDC}	1.47	1.5	1.56	V	all parameters within specification limits; IDDC ≤ 60mA	P_PMU_04_01
VDDC output voltage in LCMN or LCMA mode	V_{DDCLCM}	0.88	0.9	0.97	V	No external load; MCU in stop mode; 2.6 ≤ VDDP ≤ 5.5 V	P_PMU_04_02
VDDC output current @ High Current Mode (HCM)	I_{DDCHCM}	0	-	60	mA	[1] only used as internal core supply and supply of internal analog modules	P_PMU_04_03
VDDC output current @ Low Current Mode (LCMN and LCMA)	I_{DDCLCM}	0	-	2.5	mA	[1] only used as internal core supply and supply of internal analog modules	P_PMU_04_04
VDDC undervoltage falling threshold	$V_{DDCUVFALL}$	1.2	1.25	1.3	V		P_PMU_04_05
VDDC undervoltage rising threshold	$V_{DDCUVRISE}$	1.23	1.28	1.33	V	[1]	P_PMU_04_06
VDDC undervoltage filter time (analog)	$t_{VDDCUVFT}$	0.85	2	4	µs	[1]	P_PMU_04_08
VDDC undervoltage warning falling threshold	$V_{DDCUVWFALL}$	1.317	1.372	1.427	V		P_PMU_04_09
VDDC undervoltage warning rising threshold	$V_{DDCUVWRISE}$	1.349	1.405	1.461	V	[1]	P_PMU_04_10
VDDC undervoltage warning filter time	$t_{VDDCUVWFT}$	27	32	37	µs	[1]	P_PMU_04_11
VDDC overvoltage falling threshold	$V_{DDCOVFALL}$	1.62	1.69	1.76	V	[1] V_S > 3V	P_PMU_04_12
VDDC overvoltage rising threshold	$V_{DDCOVRISE}$	1.65	1.72	1.79	V		P_PMU_04_13
VDDC overvoltage filter time	$t_{VDDCOVFT}$	1	2	3	µs	[1]	P_PMU_04_14
VDDC overcurrent falling threshold	$I_{DDCOCFALL}$	70	90	120	mA	[1]	P_PMU_04_15

Table 25 VDDC DC Specification (cont'd)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VDDC overcurrent rising threshold	$I_{DDCOCRISE}$	80	100	130	mA		P_PMU_04_16
VDDC overcurrent filter time	$t_{VDDCOCFT}$	27	32	37	µs	[1]	P_PMU_04_17
VDDC current limitation	$I_{VDDCILIM}$	110	-	180	mA	[1] current flowing out of the pin, V_{DDC} = 0 V	P_PMU_04_19
Required VDDC output buffer capacitance	C_{VDDC}	0.57	-	2	µF	[1] ESR ≤ 0.1Ω; the specified capacitor value is a value including tolerances	P_PMU_04_21
VDDC_REG current consumption@LCM, adaptive on	$I_{VDDCREGLCMAON}$	-	-	23	µA	[1] -40°C<T_J<85°C	PH_PMU_04_23
VDDC under-voltage falling threshold 0.9 V mode	$V_{DDCUV0V9FALL}$	762	793	825	mV	V_S>3V	PH_PMU_04_24
VDDC under-voltage rising threshold 0.9 V mode	$V_{DDCUV0V9RISE}$	792	823	855	mV	V_S>3V	PH_PMU_04_25
VDDC_REG current consumption@LCM, adaptive off	$I_{VDDCREGLCMAOFF}$	-	-	20	µA	[1] -40°C<T_J<85°C	PH_PMU_04_31

[1] Not subject to production test, specified by design

5.3.2.4 VDDEXT characteristics

Table 26 VDDEXT DC Specification

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
External Sensor Supply Regulator output voltage	$V_{DDEXTILIM}$	4.9	5	5.1	V	I_{DDEXT}≤20mA	P_PMU_05_14
External Sensor Supply Regulator output voltage	$V_{DDEXTTLIM}$	4.9	5	5.1	V	I_{DDEXT}=40mA; -40°C≤T_J≤150°C	P_PMU_05_15

Table 26 VDDEXT DC Specification (cont'd)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	**Symbol**	**Values**			**Unit**	**Note or Test Condition**	**Number**
		Min.	**Typ.**	**Max.**			
External Sensor Supply Regulator output voltage	V_{DDEXT}	4.8	5	5.2	V	-40°C≤T_J≤175°C	P_PMU_05_01
VDDEXT voltage drop with respect to V_S	$V_{DDEXTDROP}$	0	50	300	mV	0mA≤I_{DDEXT}≤20mA; 3V≤V_S≤5V	P_PMU_05_02
VDDEXT output current	I_{DDEXT}	0	-	40	mA	[1]	P_PMU_05_03
VDDEXT load regulation	$V_{DDEXTLOR}$	-100	-	10	mV	[1] 0mA≤I_{DDEXT}≤40mA	P_PMU_05_16
VDDEXT dynamic load regulation	$V_{DDEXTLOR\_DYN}$	-130	-	50	mV	[1] I_{DDEXT} jumping from 0mA to 40mA and from 40mA to 0mA with Δl/Δt=40mA/µs	P_PMU_05_17
VDDEXT line regulation	$V_{DDEXTLIR}$	-60	-	60	mV	[1] 0mA≤I_{DDEXT}≤40mA	P_PMU_05_18
VDDEXT dynamic line regulation	$V_{DDEXTLIR\_DYN}$	-500	-	500	mV	[1] V_S jumping from 5.5V to 18V and from 18V to 5.5V with ΔV/Δt=5V/µs	P_PMU_05_19
VDDEXT output discharge resistance	R_{VDDEXT_DISCHG}	16	20	24	kΩ	I_{VDDEXT} = 0.2mA, MCU in active state, VDDEXT_CTRL=[00000000]h	P_PMU_05_20
VDDEXT undervoltage shutdown threshold	$V_{DDEXTUV}$	1.55	1.9	2.1	V		P_PMU_05_04
VDDEXT undervoltage filter time	$t_{VDDEXTUVFT}$	6	8	10	µs	[1]	P_PMU_05_05
VDDEXT current limitation	$I_{DDEXTILIM}$	100	250	380	mA	[1] current flowing out of the pin, V_{DDEXT} = 0 V	P_PMU_05_06
VDDEXT overtemperature threshold	$T_{jVDDEXTOTSHD}$	180	200	215	°C	[1]	P_PMU_05_07
VDDEXT overtemperature filter time	$t_{VDDEXTOTFT}$	8	10	12	µs	[1]	P_PMU_05_08

Table 26 VDDEXT DC Specification (cont'd)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VDDEXT ripple rejection 1	$PSRR_{VDDEXT1}$	50	-	-	dB	[1] @0mA≤Iload≤20mA; @2Vpp @Vs=13.5V @ 0kHz<f≤1kHz	P_PMU_05_09
VDDEXT ripple rejection 2	$PSRR_{VDDEXT2}$	38	-	-	dB	[1] @2Vpp @Vs=13.5V; @1kHz≤f≤10kHz	P_PMU_05_10
VDDEXT ripple rejection 3	$PSRR_{VDDEXT3}$	26	-	-	dB	[1] @0.5Vpp @Vs=13.5V; @10kHz≤f≤20kHz	P_PMU_05_11
Required VDDEXT output buffer capacitance	C_{VDDEXT}	0.43	-	2	µF	[1] ESR < 0.1Ω; the specified capacitor value is a value including tolerances	P_PMU_05_13

[1] Not subject to production test, specified by design

5.3.3 Clock Generators

5.3.3.1 Master clock characteristics

Table 27 Master Clock Specification

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Master clock frequency	f_{MCLK}	17	20	23	MHz		P_PMU_06_01
Master clock settling time	$t_{MCLKRDY}$	0.8	1	1.2	µs	[1]	P_PMU_06_03
Master clock failure detection time	$t_{MCLKWDGFT}$	20	30	40	µs	[1] Timing is refered to REFCLK	P_PMU_06_04

1) Not subject to production test, specified by design

5.3.3.2 Safe reference clock characteristics

Table 28 Safe Reference Clock Specification

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Safe reference clock frequency	$f_{SAFERCLK}$	85	100	115	kHz		P_PMU_07_01
Safe reference clock settling time	$t_{SAFERCLKRDY}$	40	50	60	µs	[1]	P_PMU_07_03

1) Not subject to production test, specified by design

5.3.4 System state control

Table 29 System State Control

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reset pin input filter time	T_{filt_RESET}	80	100	120	µs	Filter time starts when the configurable blanking/blind time expired	P_PMU_11_01
MONx wake source filter time	t_{MONx_FT}	27.2	32	36.8	µs	1) Two values configurable	P_PMU_08_01
Port0.x wake source filter time	t_{PORT0_x}	27.2	32	36.8	µs	1)	P_PMU_08_02
Port1.x wake source filter time	t_{PORT1_x}	27.2	32	36.8	µs	1)	P_PMU_08_03
Port2.x wake source filter time	t_{PORT2_x}	27.2	32	36.8	µs	1)	P_PMU_08_04
Fail-Safe Sleep VDDP_TMOUT trigger timeout	$t_{VDDPUVTO}$	0.8	1	1.2	ms	1)	P_PMU_08_05
Fail-Safe Sleep VDDC_TMOUT trigger timeout	$t_{VDDCUVTO}$	400	500	600	µs	1)	P_PMU_08_06
Fail-Safe Sleep SYSTEM_CLK_WDG _FAIL	$t_{LOSSFSYSFT}$	27.2	32	36.8	µs	1)	P_PMU_08_07
Fail-Safe Sleep SYSTEM_OT filter time	$t_{SYSOTFT}$	27.2	32	36.8	µs	1)	P_PMU_08_08
Fail-Safe Sleep SAFE_WDT _FAIL	$t_{FSWDTFT}$	27.2	32	36.8	µs	1)	P_PMU_08_09

1) Not subject to production test, specified by design

5.3.5 FIFO Fail-safe supervision

Table 30 FIFO Fail Safe Supervision

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	**Symbol**	**Values**			**Unit**	**Note or Test Condition**	**Number**
		Min.	**Typ.**	**Max.**			
Fail safe output low voltage	$V_{FO,L}$	-	0.6	1	V	$I_{FO} < 4mA$	P_PMU_10_01
Fail Safe input leakage current	$I_{FO,LK}$	-	-	2	µA	$V_{FO} < 28V$	P_PMU_10_02
Fail-safe input threshold voltage	V_{FIth}	2	3	3.8	V		P_PMU_10_03
Fail safe input threshold hysteresis	$V_{FIth,hys}$	0.1	-	0.7	V		P_PMU_10_04
Fail-safe input filter time	$t_{FI,filt}$	6	8	10	µs	[1]	P_PMU_10_05
Fail-safe input pull-up resistor	$R_{FI,PU}$	30	40	50	kΩ	[1] Switchable resistor to V_S	P_PMU_10_06

1) Not subject to production test, specified by design

5.3.6 Monitoring and supply generation

Table 31 Monitoring Reference and Supply Generation Specification

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PMU Failsafe Analog current consumption in sleep mode	$I_{PMUFSSLEEP}$	-	-	10	µA	[1] Only VMON_SUP_REF and VMSUP_MON active; -40°C<T_j<85°C	PH_PMU_10_01

1) Not subject to production test, specified by design

Table 32 VAREF Monitoring Specification

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VAREF over-voltage rising threshold	$V_{AREFOVRISE}$	5.4	5.63	5.85	V		PH_PMU_11_02
VAREF over-voltage threshold hysteresis	$V_{AREFOVHST}$	-	100	-	mV	[1]	PH_PMU_11_03

1) Not subject to production test, specified by design

6 System Control Unit (SCU)

6.1 Features overview

The SCU provides following features:

- Flexible clock management with different clock sources and prescaler options. This allows a high flexibility for the operation modes and ensures a fail-safe behavior in case of a clock failure
- Flexible peripheral management when enabling and disabling peripherals, when switching the system states and when debugging. The SCU supports the shutdown for some peripherals and the whole system in case of a critical system state
- The assignment of interrupt and exception request events to the NVIC and DMA request events to the DMA module is done inside the SCU

6.2 Block diagram

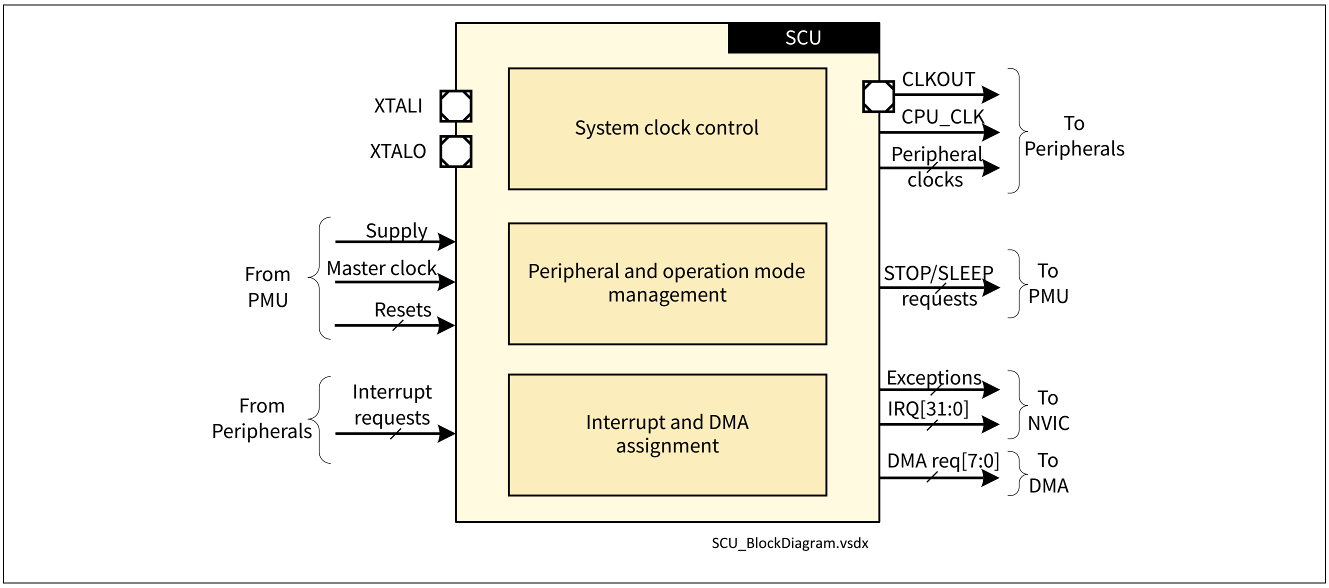


Figure 10 **Block diagram SCU**

6.3 Electrical characteristics SCU

6.3.1 Oscillators and PLL characteristics

The following table contains the ECs of all system oscillators and the integrated PLL.

Table 33 HP_CLK Oscillator (SCU Clock Control)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	**Symbol**	**Values**			**Unit**	**Note or Test Condition**	**Number**
		Min.	**Typ.**	**Max.**			
HP_CLK frequency range	f_{HP}	78.4	80	81.6	MHz	This is the f_{HP} frequency range over all operating conditions	P_SCU_02_02
HP_CLK short term frequency deviation	f_{HPST}	-0.4%	-	0.4%	MHz	frequency deviation of f_{HP} within 100 ms, incl. VDDC variation (VDDCmin and VDDCmax) and temperature variation of 30 K	P_SCU_02_03
HP_CLK Start-up time	t_{HPUP}	-	-	1	µs	(1) from power supply stable	P_SCU_02_04

1) Not subject to production test, specified by design

Table 34 PLL0

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	**Symbol**	**Values**			**Unit**	**Note or Test Condition**	**Number**
		Min.	**Typ.**	**Max.**			
VCO reference frequency range	f_{REF0}	0.8	1	1.27	MHz	(1) fref0 = fin0/PDIV0	P_SCU_03_01
VCO frequency (tuning) range	f_{VCO0}	48	-	160	MHz	(1)	P_SCU_03_02
Input frequency range	f_{in0}	4	-	40	MHz	(1)	P_SCU_03_03
Output frequency range	f_{PLL0}	5	-	80	MHz	(1)	P_SCU_03_04
Free-running frequency	$f_{VCOfree0}$	10	21.5	45	MHz	(1)	P_SCU_03_05

Table 34 PLL0 (cont'd)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Accumulated jitter with external oscillator	t_{jacc0}	-5	-	5	ns	[1] accumulated over 300 cycles; @f_{PLL0} = 60 MHz, NDIV = 120, PDIV = 2; f_{XTAL} = 16 MHz	P_SCU_03_06
Lock-in time	t_{L0}	-	-	260	µs	[1] from enable till lock	P_SCU_03_07

1) Not subject to production test, specified by design

Table 35 PLL1

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VCO reference frequency range	f_{REF1}	0.8	1	1.27	MHz	[1] fref1 = fin1/PDIV1	P_SCU_04_01
VCO frequency (tuning) range	f_{VCO1}	48	-	160	MHz	[1]	P_SCU_04_02
Input frequency range	f_{in1}	4	-	40	MHz	[1]	P_SCU_04_03
Output frequency range	f_{PLL1}	5	-	80	MHz	[1]	P_SCU_04_04
Free-running frequency	$f_{VCOfree1}$	10	21.5	45	MHz	[1]	P_SCU_04_05
Accumulated jitter with external oscillator	t_{jacc1}	-5	-	5	ns	[1] accumulated over 300 cycles; @f_{PLL1} = 80 MHz, NDIV = 160, PDIV = 2; f_{XTAL} = 16 MHz	P_SCU_04_06
Lock-in time	t_{L1}	-	-	260	µs	[1] from enable till lock	P_SCU_04_07

1) Not subject to production test, specified by design

Table 36 Current consumption

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PLLx active current	IDD_{PLL}	-	-	1	mA	[1] @ f_{PLL} = 20 to 80 MHz	P_SCU_05_01

1) Not subject to production test, specified by design

6.3.2 External clock characteristics (XTAL1, XTAL2)

Table 37 Functional Range

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range for signal on XTALI	V_{IXI}	-0.2	-	1.7	V	[1]	P_SCU_06_01
Input amplitude on XTALI	V_{AXI}	0.6	-	-	V	[1] Peak-to-peak voltage	P_SCU_06_02
XTALI input current	I_{IL}	-20	-	20	µA	[1] $0V<V_{IN}<V_{DDC}$	P_SCU_06_03
Digital oscillator input frequency	f_{XTALI}	4	-	40	MHz	[2] [1] on XTALI	P_SCU_06_04
Analog oscillator input frequency	f_{XTAL}	4	-	16	MHz	[1] connected to XTALI/XTALO	P_SCU_06_05
XTALI high time	t_1	6	-	-	ns	[1] this is a system requirement and must be ensured by application	P_SCU_06_06
XTALI low time	t_2	6	-	-	ns	[1] this is a system requirement and must be ensured by application	P_SCU_06_07
XTALI rise time	t_3	-	-	8	ns	[1] this is a system requirement and must be ensured by application; 10% to 90%	P_SCU_06_08
XTALI fall time	t_4	-	-	8	ns	[1] this is a system requirement and must be ensured by application; 90% to 10%	P_SCU_06_09

1) Not subject to production test, specified by design

2) Above 24MHz the hysteresis needs to be switched off (see register SCU_XTAL_CTRL).

7 Microcontroller Unit (MCU)

7.1 Features overview

The MCU provides following features:

- Arm® Cortex®-M3 processor
  - Arm® Cortex®-M3 processor core
  - Arm® System Timer (SYSTICK)
  - Nested Vector Interrupt Controller (NVIC)
  - Arm® CoreSight™ Debug Unit (SW-DP)
- Direct Memory Access (DMA)
- Memory system
  - Non-volatile memory uncached (FLASH0)
  - Non-volatile memory cached (FLASH1)
  - Program SRAM memory (PSRAM)
  - Data SRAM memory (DSRAM)
  - Read-only memory (ROM)
- Cache system
- Multilayer Bus Matrix
  - Bus Matrix interconnect topology
  - AHB watcher
- Memory Access Control (MAC)
  - Memory protection
  - Trusted Gate mechanism
  - Firmware
- Peripheral Bridge (PBA0/1)

7.2 Block diagram

The **Figure 11** illustrates the top-level architecture of the Microcontroller Unit sub-system.

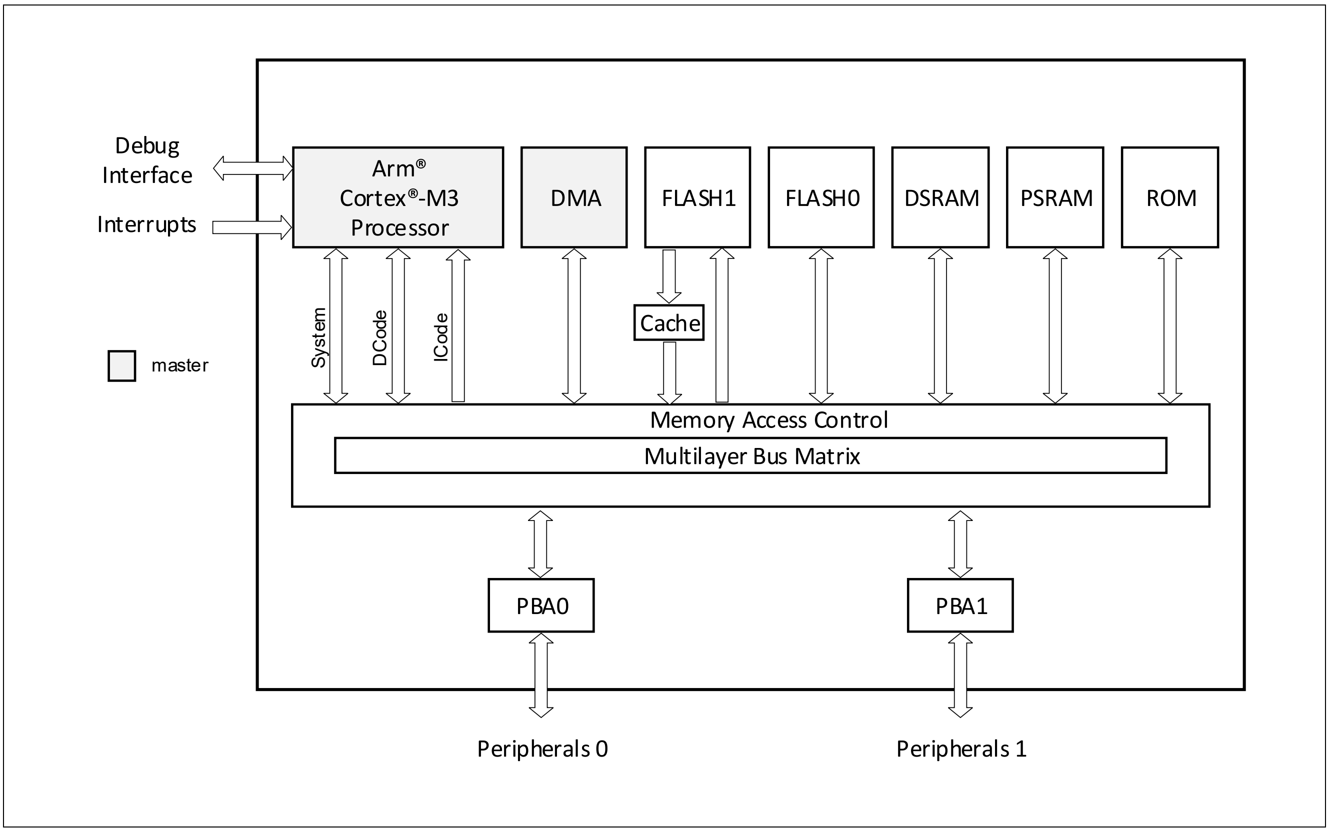


Figure 11 Block diagram MCU

7.3 Electrical characteristics Flash parameters

7.3.1 FLASH0 and FLASH1 characteristics

This chapter includes the parameters of the embedded flash module (incl. config sector).

Table 38 Flash Characteristics

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Read time	t_{read_ac}	-	-	75	ns	Read accesses to the flash module which is under write/erase/verify operation is not allowed; 3V≤V_s≤28V	P_NVM_01_01
Programming time per 128 Byte page	t_{PR}	-	3	3.5	ms	3V≤V_s≤28V	P_NVM_01_02
Programming time per 128 Byte page incl. Firmware routine runtime for program operation	t_{PR_FW}	-	-	4	ms	3V≤V_s≤28V	P_NVM_01_03
Erase time per sector/page	t_{ER}	-	4	4.5	ms	3V≤V_s≤28V	P_NVM_01_04
Erase time per sector/page incl. Firmware routine runtime for erase operation	t_{ER_FW}	-	-	5	ms	3V≤V_s≤28V	P_NVM_01_05
Data retention time	t_{RET}	20	-	-	years	@N_{ER}	P_NVM_01_06
Data retention time for device storage	t_{RET_strg}	50	-	-	years	[1] [2] @N_{ER}; T_j=30°C	P_NVM_01_07
Flash endurance for page within user sectors for FLASH0	N_{ER_high}	30	-	-	kcycles	Valid for FLASH0	P_NVM_01_08
Flash erase endurance for security pages	N_{SEC}	10	-	-	cycles	Data retention time 20 years; T_j=25°C	P_NVM_01_09
Drain disturb limit	N_{DD}	32	-	-	kcycles	[3]	P_NVM_01_10

Table 38 Flash Characteristics (cont'd)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Flash endurance for page within user sectors for FLASH0/1	N_{ER}	1	-	-	kcycles	Valid for FLASH0 and FLASH1	P_NVM_01_11
Data retention time for high endurance	t_{RET_short}	5	-	-	years	@N_{ER_high}	P_NVM_01_12

1) Derived by extrapolation of lifetime tests.

2) Not subject to production test, specified by design

3) This parameter limits the number of subsequent programming operations within a physical sector without a given page in this sector being (re-)programmed. The drain disturb limit is applicable if wordline erase is used repeatedly. For normal sector erase/program cycles this limit will not be violated. For data sectors the integrated EEPROM emulation firmware routines handle this limit automatically, for wordline erases in code sectors (without EEPROM emulation) it is recommended to execute a software based refresh, which may make use of the integrated random number generator NVMBRNG to statistically start a refresh.

8 System Watchdog Timer (SYSWDT)

8.1 Features overview

The System Watchdog Timer (SYSWDT) belongs to the MCU subsystem. The SYSWDT resets the MCU subsystem in case it is not serviced within a defined time. Therefore it can bring the system into a defined state if the software is not executing according to its normal timing scheme due to a malfunction.

The SYSWDT provides following features:

- 16-bit window watchdog timer
- Programmable watchdog period and window
- Selectable input frequency
- Prewarning interrupt for debug purpose

8.2 Block diagram

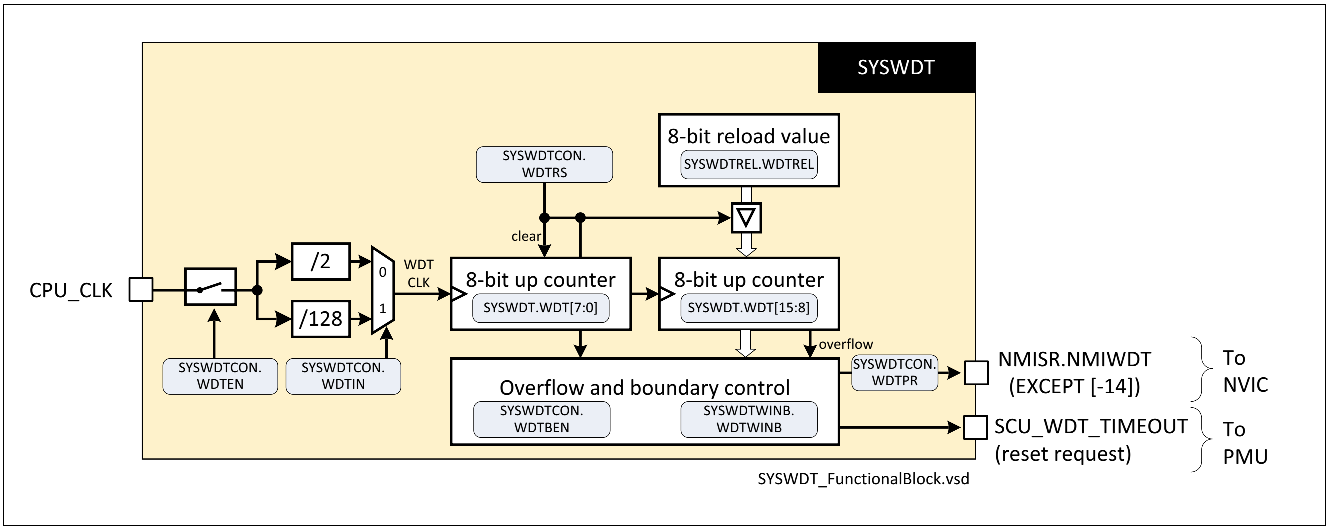


Figure 12 Block diagram SYSWDT

9 Universal Asynchronous Receiver Transmitter (UART0/1)

9.1 Features overview

The UART0/1 provide a full-duplex asynchronous receiver/transmitter, i.e., it can transmit and receive simultaneously. They are also receive-buffered (1 byte), i.e., they can commence reception of further bytes before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time the reception of the second byte is complete, the previous byte will be lost. The serial port receive and transmit registers are accessed at Special Function Register (SFR) TXBUF and RXBUF. Writing to TXBUF loads the transmit register, and reading RXBUF accesses a physically separate receive register.

The UART0/1 provides following features:

- Full-duplex asynchronous modes
  - 8-bit or 9-bit data frames, LSB first
  - fixed or variable baud-rate
- Receive buffered (1 Byte)
- Transmit buffered (1 Byte)
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception
- Baud-rate generator with fractional divider for generating a wide range of baud-rates, e.g. 9.6 kBaud, 19.2 kBaud, 115.2 kBaud, 125 kBaud, 250 kBaud, 500 kBaud, 2 MBaud
- Hardware logic for break and synch Byte detection
- Tx inverter logic
- LIN support: connected to timer channel for synchronization to LIN baud-rate

In all modes, transmission is initiated by any instruction that uses TXBUF as a destination register or by writing to the start bit or by an external event. The start selection is programmable. Reception is initiated in the modes by the incoming start bit if REN = 1.

The serial interface also provides interrupt requests when transmission or reception of the frames has been completed. The corresponding interrupt request flags are TI or RI, respectively. If the serial interrupt is not used (i.e., serial interrupt not enabled), TI and RI can also be used for polling the serial interface.

9.2 Block diagram

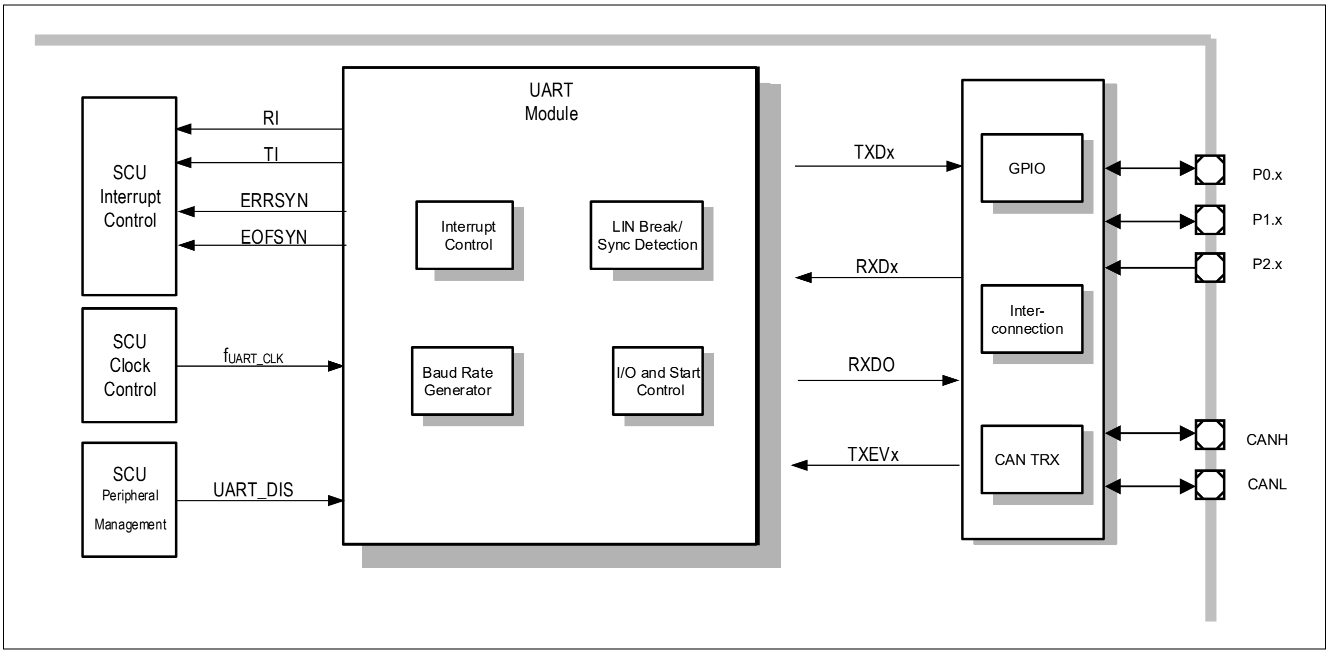


Figure 13 Block diagram UART

10 High-Speed Synchronous Serial Interface (SSC0/1)

10.1 Features overview

The two high-speed synchronous serial interfaces SSC0/1 support both full-duplex and half-duplex serial synchronous communication.

The SSC0/1 provides following features:

- Master and Slave Mode operation
  - Full-duplex or half-duplex operation
- Transmit and receive buffered
- Flexible data format
  - Programmable number of data bits: 2 to 64-bits
  - Programmable shift direction: Least Significant Bit (LSB) or Most Significant Bit (MSB) shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud-rate, up to 15 MBaud (Slave mode), 30 MBaud (Master Mode)
- Chip Select (Master), for 1 … 4 slaves
- Chip Select (Slave)
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
  - Interrupt on a transmitter empty condition
  - Interrupt on a receiver full condition
  - Interrupt on an error condition (receive, phase, baud-rate, transmit error)

10.2 Block diagram

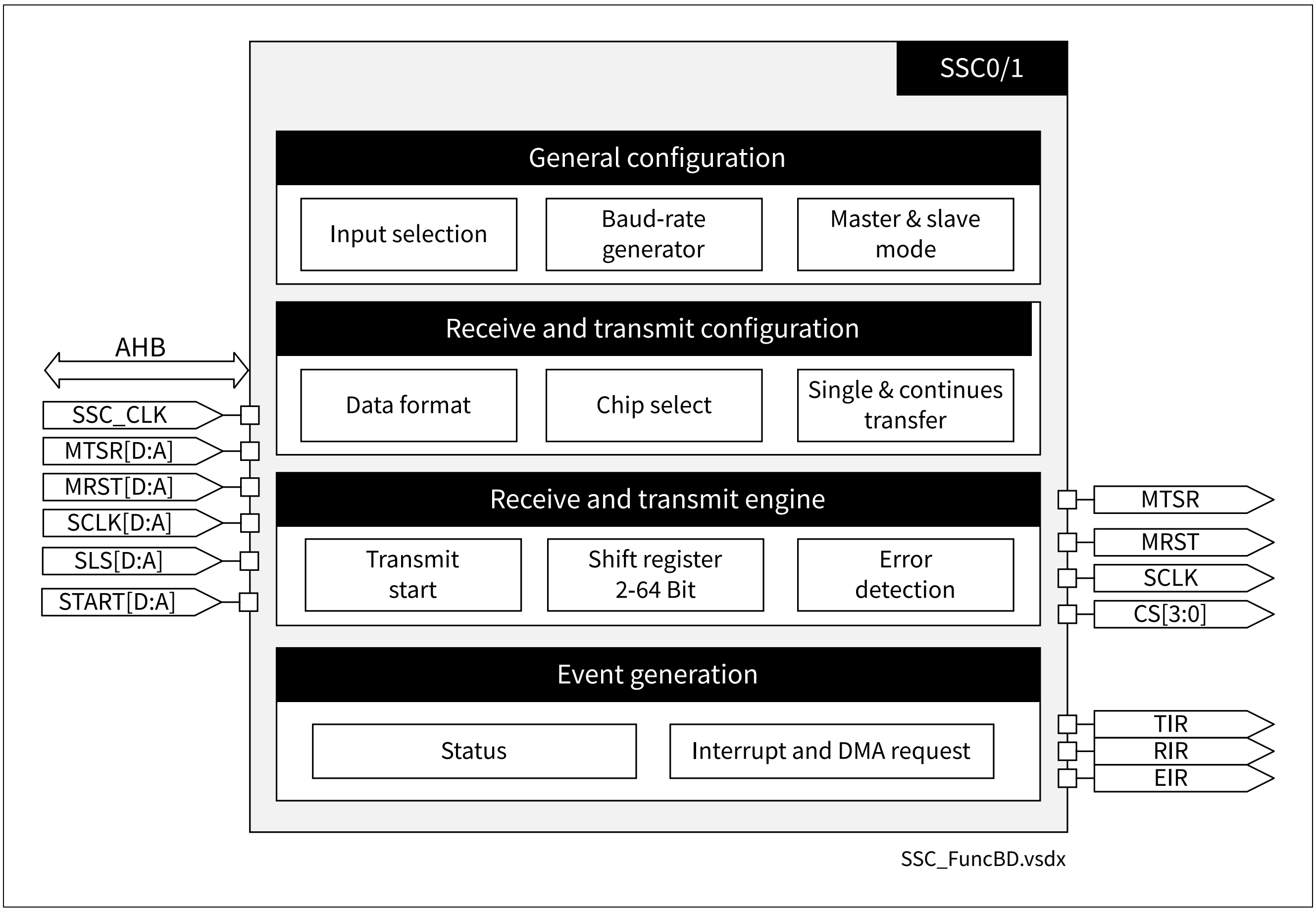


Figure 14 Block diagram SSC

10.3 Electrical characteristics SSC0/1

10.3.1 SSC timing characteristics

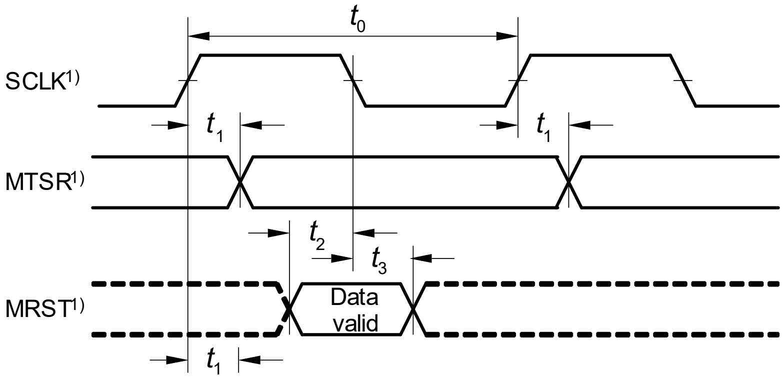
Table 39 SSC Master Mode Timing (Operating Conditions apply, CL = 50 pF)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SCLK clock period	t_0	2 * T_{SSC}	-	-		[1] [2] V_{DDP}>2.7V	P_SSC_01_01
MTSR delay from SCLK	t_1	10	-	-	ns	[2] V_{DDP}>2.7V	P_SSC_01_02
MRST setup to SCLK	t_2	10	-	-	ns	[2] V_{DDP}>2.7V	P_SSC_01_03
MRST hold from SCLK	t_3	15	-	-	ns	[2] V_{DDP}>2.7V	P_SSC_01_04

1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$.
If f_{CPU} = 20 MHz, t_0 = 100 ns. T_{CPU} is the CPU clock period. Additionally, the speed limitation of the GPIO needs to be taken into account.

2) Not subject to production test, specified by design



1) This timing is based on the following setup: CON.PH = CON.PO = 0.

SSC_Tmg1

Figure 15 SSC master mode timing

11 CAN Controller (MultiCAN+)

11.1 Features overview

The MultiCAN+ provides a communication interface which is compliant to the CAN specification CAN FD ISO11898-1 (non-ISO CAN FD format and ISO CAN FD), providing communications at up to 1 Mbit/s in classical CAN (ISO 11898-1:2003(E) mode and/or CAN FD until 2 MBaud data speed, dependent on frequency and nodes).

The MultiCAN+ for the TLE989x/TLE988x consists of 1 module (i.e. MultiCAN with 1 CAN nodes), representing 1 serial communication interfaces. All nodes are CAN FD capable. Each CAN node communicates over two pins (TXD and RXD). The device ports which are used for TXD and RXD may be individually configured within the GPIO block. Several port configuration options are available to provide application-specific flexibility.

The MultiCAN+ contains 1 independently operating CAN node with Full-CAN functionality that is able to exchange Data and Remote Frames via a gateway function. Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of 32 message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to the message object list of the CAN node, and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

The bit timings for the CAN nodes are derived from the module timer clock (f_{CAN}) and are programmable up to a data rate of 1 Mbit/s in Classical CAN (ISO 11898-1:2003(E) mode or up to 2 MBaud in CAN FD mode. External bus transceivers are connected to a CAN node via a pair of receive and transmit pins.

The MultiCAN+ provides the following features:

- Compliant with ISO 11898 and SAE J 1939
- Supports CAN with Flexible Data-Rate Specification CAN FD (non-ISO CAN FD format and ISO CAN FD) with max. 64 data bytes
- Data transfer rates up to 1 Mbit/s when operating in Classical CAN mode per ISO 11898-1:2003(E)
- Supports up to 2 MBaud, when operating in CAN FD mode.
- Support for asynchronous clock sources for baud-rate generation
- Flexible and powerful message transfer control and error handling capabilities
- Advanced CAN bus bit timing analysis and baud-rate detection for each CAN node via a frame counter
- Full-CAN functionality: A set of 32 message objects can be individually
  - Configured as transmit or receive object
  - Setup to handle frames with 11-bit or 29-bit identifier
  - Identified by a timestamp via a frame counter
  - Configured to remote monitoring mode
- Advanced Acceptance Filtering
  - Each message object provides an individual acceptance mask to filter incoming frames
  - A message object can be configured to accept standard or extended frames or to accept both standard and extended frames
  - Message objects can be grouped into different priority classes for transmission and reception

  - The selection of the message to be transmitted first can be based on frame identifier, IDE bit and RTR bit according to CAN arbitration rules, or on its order in the list
- Advanced CAN node features
  - Analyzer mode supports monitoring of bus traffic without actively participating on the bus
  - Internal Loop-Back mode is available for test purposes
  - Data transmission from a node can be stopped without affecting reception
  - Programmable minimum delay between two consecutive messages
- Advanced message object functionality
  - Message objects can be combined to build FIFO message buffers of arbitrary size, limited only by the total number of message objects
- Advanced data management
  - The message objects are organized in double-chained lists
  - up to 8 lists can be used for message objects
  - List reorganizations can be performed at any time, even during full operation of the CAN nodes
  - A powerful, command-driven list controller manages the organization of the list structure and ensures consistency of the list
  - Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation
- Advanced interrupt handling
  - Message interrupts, node interrupts can be generated
  - Interrupt requests can be routed individually to one of the 3 interrupt output lines
  - Message post-processing notifications can be combined flexibly into a dedicated register field of 256 notification bits

11.2 Block diagram

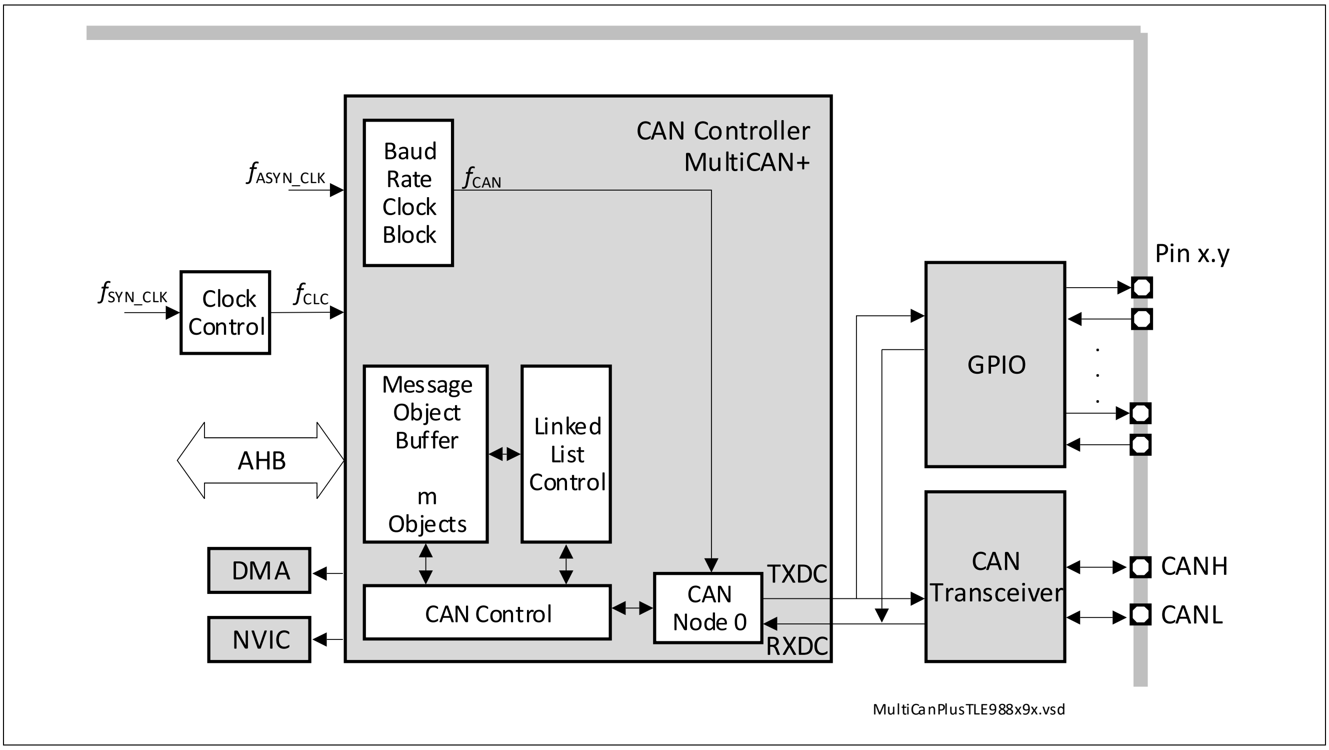


Figure 16 **Block diagram MultiCAN+**

12 CAN Transceiver (CANTRX)

12.1 Features overview

The CAN transceiver (CANTRX) meets the physical layer requirements of the ISO11898-2:2016 High-Speed Controller Area Network (CAN) specification providing an interface between the CAN bus and the CAN protocol controller (MultiCAN+).

The CANTRX provides following features:

- Compliant to ISO11898-2:2016
- Compliant to classical CAN and CAN-FD up to 5 Mbps
- Fulfills CAN interfaces (v1.2) OEM hardware requirements
- Supports four operating modes:
  - Off mode
  - Normal mode (Rx, Tx)
  - Receive-only mode (Rx-only)
  - Sleep mode for low-power operation. Wake-up time: <100 µs typ. Wake-up pattern recognition
- Interfaces with multiple hosts:
  - MultiCAN+ protocol controller
  - UART
  - GPIO
  - Timer GPT12 and Timer2 (T2)
- CAN bus bias control. Ideal passive behavior when unpowered.
- Diagnostics:
  - CAN supply (VCAN) undervoltage supervision
  - CAN bus dominant timeout
  - CAN transceiver input (TxD) dominant timeout
- Overtemperature protection

12.2 Block diagram

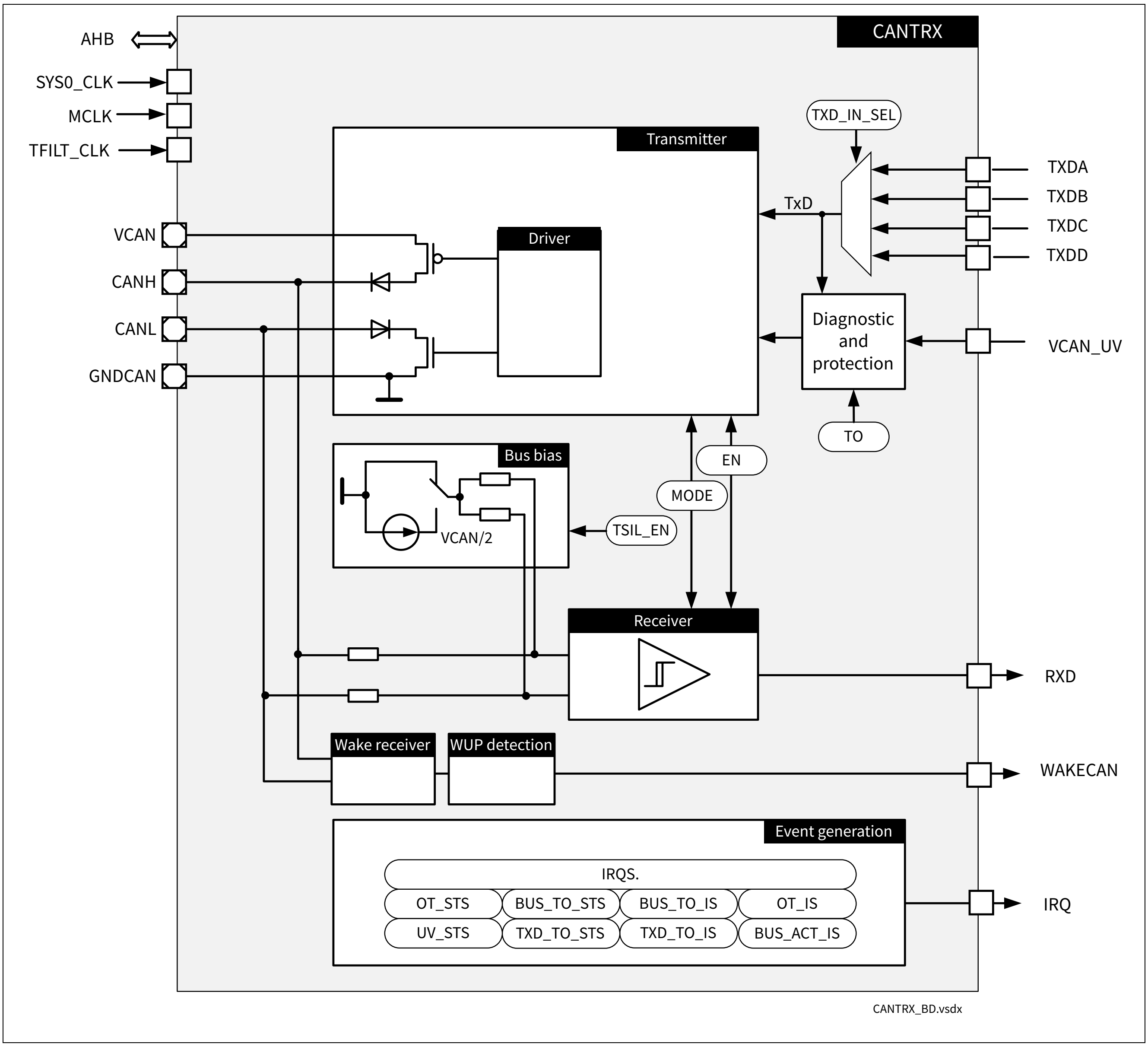


Figure 17 Block diagram CANTRX

12.3 Electrical characteristics CANTRX

12.3.1 CANTRX characteristics

Table 40 CAN Bus Receiver

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, V_{CAN} = 4.75 V to 5.25 V, R_L = 60 Ω, CAN Normal mode, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
"Dominant" differential range	V_{diff, D_range}	0.9	-	8.0	V	CAN Normal/Receive-only Mode; -12V≤V_{CM}(CAN)≤12V; V_{diff}=V_{CANH} - V_{CANL}	P_CAN_01_01
"Recessive" differential range	V_{diff, R_range}	-3.0	-	0.5	V	CAN Normal/Receive-only Mode; -12V≤V_{CM}(CAN)≤12V; V_{diff}=V_{CANH} - V_{CANL}	P_CAN_01_02
Common Mode Range	*CMR*	-12	-	12	V	[1]	P_CAN_01_03
CANH, CANL Input Resistance	R_{in}	20	40	50	kΩ	Recessive state; -2V≤$V_{CANL/H}$≤7V	P_CAN_01_04
Differential Input Resistance	R_{in_diff}	40	80	100	kΩ	Recessive state; -2V≤$V_{CANL/H}$≤7V	P_CAN_01_05
Input Resistance Deviation between CANH and CANL	DR_i	-3	-	3	%	[1] Recessive state; V_{CANL}=V_{CANH} = 5V	P_CAN_01_06
Input Capacitance CANH, CANL versus GND	C_{in}	-	20	40	pF	[1] Recessive state; S2P method @ f=10MHz	P_CAN_01_07
Differential Input Capacitance	C_{in_diff}	-	10	20	pF	[1] Recessive state; S2P method @ f=10MHz	P_CAN_01_08
"Dominant" differential range, CAN Sleep Mode	V_{diff,D_range_sleep}	1.15	-	8.0	V	CAN Sleep Mode; -12V≤V_{CM}(CAN)≤12V; V_{diff}=V_{CANH} - V_{CANL}	P_CAN_01_09
"Recessive" differential range, CAN Sleep Mode	V_{diff,R_range_sleep}	-3.0	-	0.4	V	CAN Sleep Mode; -12V≤V_{CM}(CAN)≤12V; V_{diff}=V_{CANH} - V_{CANL}	P_CAN_01_10

1) Not subject to production test, specified by design

Table 41 CAN Bus Transmitter

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, V_{CAN} = 4.75 V to 5.25 V, R_L = 60 Ω, CAN Normal mode, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CANH/CANL Recessive Output Voltage	V_{CANL/H_NM}	2.0	-	3.0	V	CAN Normal/Receive-only Mode; no load	P_CAN_02_01
CANH/CANL Recessive Output Voltage, CAN Sleep Mode	V_{CANL/H_LP}	-0.1	-	0.1	V	CAN Sleep Mode; no load	P_CAN_02_02
CANH, CANL Recessive Output Voltage Difference	$V_{diff\_r\_N}$	-500	-	50	mV	CAN Normal/Receive-only Mode; no load; V_{diff}=V_{CANH} - V_{CANL}	P_CAN_02_03
CANH, CANL Recessive Output Voltage Difference, CAN Sleep Mode	$V_{diff\_r\_W}$	-200	-	200	mV	CAN Sleep Mode; no load; V_{diff}=V_{CANH} - V_{CANL}	P_CAN_02_04
CANL Dominant Output Voltage	V_{CANL}	0.5	-	2.25	V	CAN Normal Mode; 50Ω≤R_L≤65Ω; V_{CAN}=5V	P_CAN_02_05
CANH Dominant Output Voltage	V_{CANH}	2.75	-	4.5	V	CAN Normal Mode; 50Ω≤R_L≤65Ω; V_{CAN}=5V	P_CAN_02_06
CANH, CANL Dominant Output Voltage Difference	$V_{diff\_d\_N}$	1.5	-	2.5	V	CAN Normal Mode; 50Ω≤R_L≤65Ω; 4.9V≤V_{CAN}≤5.25V; V_{diff}=V_{CANH} - V_{CANL}	P_CAN_02_07
CANH, CANL Dominant Output Voltage Difference (resistance during arbitration)	$V_{diff\_d\_N}$	1.5	-	5.0	V	[1] CAN Normal Mode; R_L=2240Ω; 4.9V≤V_{CAN}≤5.25V; V_{diff}=V_{CANH} - V_{CANL}	P_CAN_02_08
CANH, CANL Dominant Output Voltage Difference (extended bus load range)	$V_{diff\_d\_N}$	1.4	-	3.3	V	[1] CAN Normal Mode; 45Ω≤R_L≤70Ω; 4.9V≤V_{CAN}≤5.25V; V_{diff}=V_{CANH} - V_{CANL}	P_CAN_02_09
CANH, CANL output voltage difference slope, recessive to dominant	$V_{diff\_slope\_rd}$	-	-	70	V/µs	[1] 30% to 70% of measured differential bus voltage; C_L=100pF	P_CAN_02_14

Table 41 CAN Bus Transmitter (cont'd)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, V_{CAN} = 4.75 V to 5.25 V, R_L = 60 Ω, CAN Normal mode, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CANH, CANL output voltage difference slope, dominant to recessive	$V_{diff\_slope\_dr}$	-	-	70	V/µs	1) 70% to 30% of measured differential bus voltage; C_L=100pF	P_CAN_02_15
Driver Symmetry $V_{SYM} = V_{CANH} + V_{CANL}$	V_{SYM}	4.5	-	5.5	V	2) CAN Normal Mode; ; C_{SPLIT}=4.7nF; 50Ω≤R_L≤60Ω; V_{CAN}=5V	P_CAN_02_10
CANH Short Circuit Current	I_{CANHsc}	-115	-80	-50	mA	CAN Normal Mode; V_{CAN}=5V; $V_{CANHshort}$=-3V	P_CAN_02_11
CANL Short Circuit Current	I_{CANLsc}	50	80	115	mA	CAN Normal Mode; V_{CAN}=5V; $V_{CANLshort}$=18V	P_CAN_02_12
Leakage Current	$I_{CANH,lk}$ $I_{CANL,lk}$	-	2	5	µA	3) R_{test}=0 / 47kΩ; 0V≤$V_{CANH,L}$≤5V; V_S=V_{CAN} = 0V	P_CAN_02_13

1) Not subject to production test, specified by design

2) V_{SYM} shall be observed during dominant and recessive state and also during the transition dominant to recessive and vice versa while TXD is simulated by a square signal (50% duty cycle) with a frequency of up to 1 MHz (2 MBit/s)

3) R_{test} between (Vs/VCAN) and 0 V (GND)

Table 42 Dynamic CAN-Transceiver Characteristics

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, V_{CAN} = 4.75 V to 5.25 V, R_L = 60 Ω, CAN Normal mode, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Min. Dominant Time for Bus Wake-up	t_{Wake1}	0.5	1.2	1.8	µs	1) CAN Sleep Mode; T_J = -40°C to 85°C; -12V≤V_{CM}(CAN)≤12V	P_CAN_03_01
Wake-up Time-out, Recessive Bus	t_{Wake2}	0.8		10	ms	2) 1) CAN Sleep Mode	P_CAN_03_02
Wake-up reaction time (WUP)	t_{WU_WUP}	-	-	100	µs	3) 2) 4) 1) Wake-up reaction time after a valid WUP	P_CAN_03_03
Loop delay (recessive to dominant)	$t_{LOOP,f}$	-	150	255	ns	5) CAN Normal Mode; C_L=100pF; C_{RXD}=15pF; R_L=60Ω	P_CAN_03_04
Loop delay (dominant to recessive)	$t_{LOOP,r}$	-	150	255	ns	5) CAN Normal Mode; C_L=100pF; C_{RXD}=15pF; R_L=60Ω	P_CAN_03_05

Table 42 Dynamic CAN-Transceiver Characteristics (cont'd)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, V_{CAN} = 4.75 V to 5.25 V, R_L = 60 Ω, CAN Normal mode, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Propagation Delay TXDCAN low to bus dominant	$t_{d(L),T}$	-	90	140	ns	CAN Normal Mode; C_L=100pF; R_L=60Ω	P_CAN_03_06
Propagation Delay TXDCAN high to bus recessive	$t_{d(H),T}$	-	100	140	ns	CAN Normal Mode; C_L=100pF; R_L=60Ω	P_CAN_03_07
Propagation Delay bus dominant to RXDCAN low	$t_{d(L),R}$	-	100	140	ns	CAN Normal Mode; C_L=100pF; R_L=60Ω	P_CAN_03_08
Propagation Delay bus recessive to RXDCAN high	$t_{d(H),R}$	-	100	140	ns	CAN Normal Mode; C_L=100pF; R_L=60Ω	P_CAN_03_09
Received Recessive bit width (CAN FD up to 2Mbps)	$t_{bit(RXD)\_2M}$	400	-	550	ns	CAN Normal Mode; Parameter definition according to ISO 11898-2; C_L=100pF; C_{RXD}=15pF; R_L=60Ω; $t_{bit(TXD)}$=500ns	P_CAN_03_11
Transmitted Recessive bit width (CAN FD up to 2Mbps)	$t_{bit(BUS)\_2M}$	455	-	510	ns	CAN Normal Mode; Parameter definition according to ISO 11898-2; C_L=100pF; C_{RXD}=15pF; R_L=60Ω; $t_{bit(TXD)}$=500ns	P_CAN_03_12
Receiver timing symmetry (CAN FD up to 2Mbps)	Δt_{Rec_2M}	-45	-	15	ns	[6] CAN Normal Mode; Parameter definition according to ISO 11898-2; C_L=100pF; C_{RXD}=15pF; R_L=60Ω; $t_{bit(TXD)}$=500ns	P_CAN_03_13
Received Recessive bit width (CAN FD up to 5Mbps)	$t_{bit(RXD)\_5M}$	120	-	220	ns	CAN Normal Mode; Parameter definition according to ISO 11898-2; C_L=100pF; C_{RXD}=15pF; R_L=60Ω; $t_{bit(TXD)}$=200ns	P_CAN_03_14

Table 42 Dynamic CAN-Transceiver Characteristics (cont'd)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, V_{CAN} = 4.75 V to 5.25 V, R_L = 60 Ω, CAN Normal mode, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Transmitted Recessive bit width (CAN FD up to 5Mbps)	$t_{bit(BUS)\_5M}$	155	-	210	ns	CAN Normal Mode; Parameter definition according to ISO 11898-2; C_L=100pF; C_{RXD}=15pF; R_L=60Ω; $t_{bit(TXD)}$=200ns	P_CAN_03_15
Receiver timing symmetry (CAN FD up to 5Mbps)	Δt_{Rec_5M}	-45	-	15	ns	[6] CAN Normal Mode; Parameter definition according to ISO 11898-2; C_L=100pF; C_{RXD}=15pF; R_L=60Ω; $t_{bit(TXD)}$=200ns	P_CAN_03_16
CAN Transceiver Enabling Time	$t_{CAN,EN}$	8	12	18	µs	[2] [1] SFR "MODE" setting to first valid transmitted dominant bit	P_CAN_03_17
TXDCAN Dominant Time-out	t_{TXDCAN_TO}	1.6	2.0	2.4	ms	[2] [1] CAN Normal Mode	P_CAN_03_18
BUS Dominant Time-out	$t_{BUS\_CAN\_TO}$	2.0	2.5	3.0	ms	[2] [1] CAN Normal/Receive-only Mode	P_CAN_03_19
Time-out for bus inactivity	$t_{SILENCE}$	0.6	-	1.2	s	[2] [1]	P_CAN_03_20
Bus Bias reaction time	t_{Bias}	-	-	250	µs	[2] [1]	P_CAN_03_21

1) Not subject to production test, specified by design
2) Tolerance defined by internal oscillator tolerance
3) Wake-up is signalized via VDDC ramping up
4) For WUP: time starts with end of last dominant phase of WUP
5) V_{SYM} shall be observed during dominant and recessive state and also during the transition dominant to recessive and vice versa while TXD is simulated by a square signal (50% duty cycle) with a frequency of up to 1 MHz (2 MBit/s)
6) $\Delta t_{Rec} = t_{bit(RXD)} - t_{bit(BUS)}$

Table 43 CAN Overtemperature Characteristics

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, V_{CAN} = 4.75 V to 5.25 V, R_L = 60 Ω, CAN Normal mode, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CAN overtemperature threshold	T_{jCAN_OT}	175	185	195	°C	[1]	P_CAN_04_01
CAN overtemperature hysteresis	$T_{jCAN\_OT,hys}$	-	10	-	K	[1]	P_CAN_04_02
CAN overtemperature filter time	$t_{CAN\_OT\_FT}$	4	5	6	µs	[1]	P_CAN_04_03

[1] Not subject to production test, specified by design

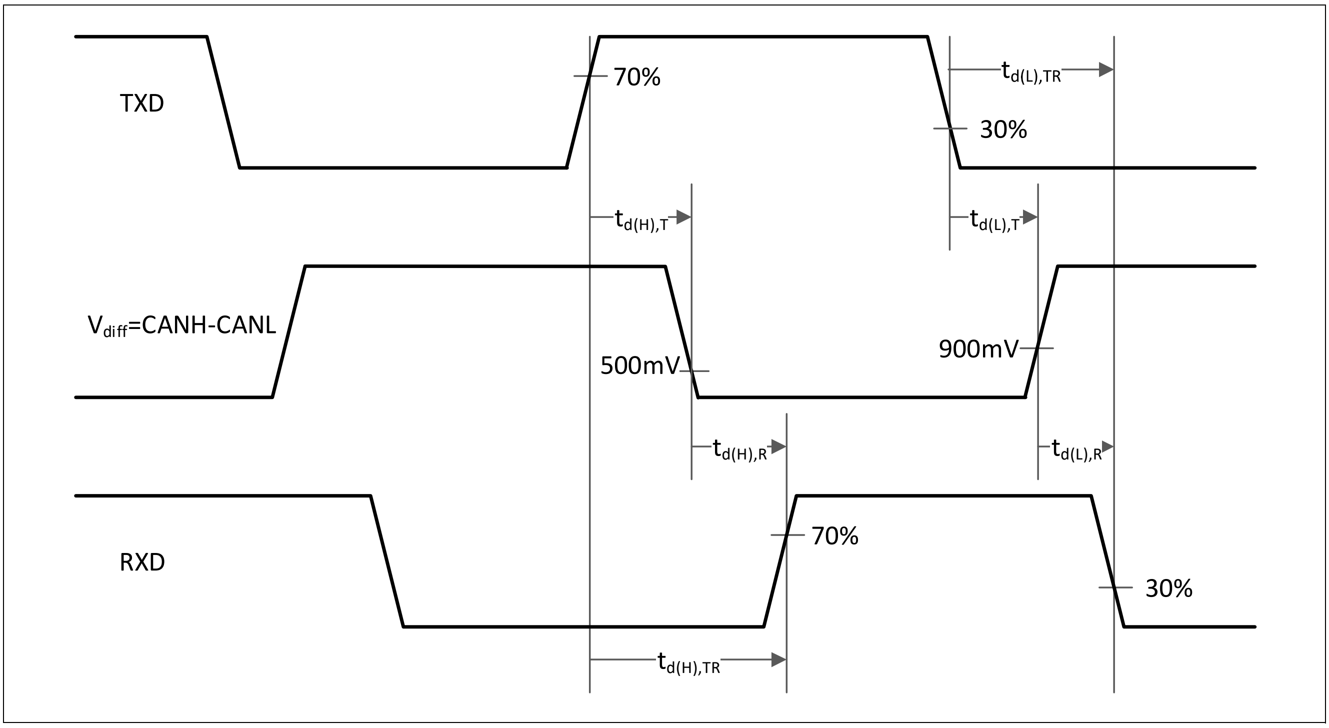


Figure 18 Timing diagrams for dynamic characteristics

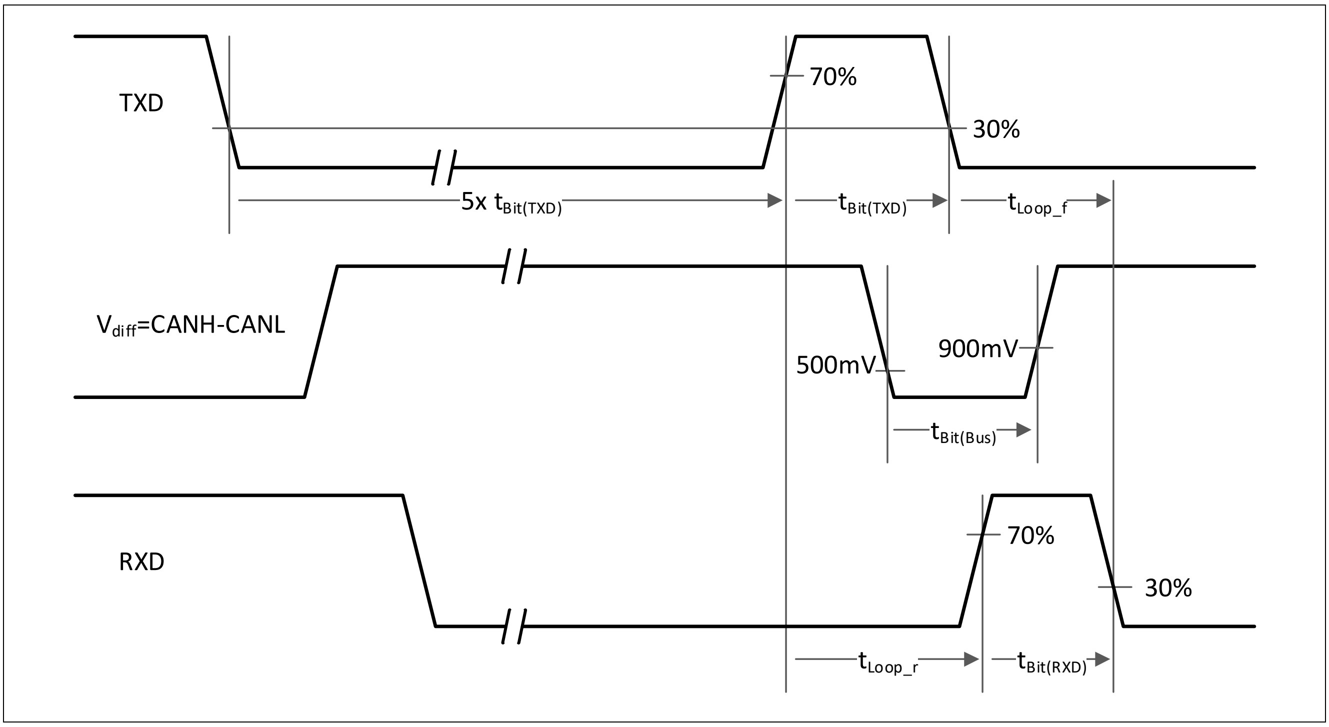


Figure 19 From ISO 11898-2: t_{loop}, $t_{\mathrm{bit(TXD)}}$, $t_{\mathrm{bit(Bus)}}$, $t_{\mathrm{bit(RXD)}}$ definitions

13 General Purpose Ports (GPIO)

13.1 Features overview

The TLE989x/TLE988x has many digital port pins, which can be used as General Purpose I/Os (GPIO) and are connected to the on-chip peripheral units.

The TLE989x/TLE988x has port pins organized into three parallel ports: Port 0 (P0), Port 1 (P1) and Port 2 (P2). Each port pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. P0 and P1 are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected. On Port 2 (P2) analog inputs are shared with general purpose digital inputs.

The GPIOs provide a generic and flexible software and hardware interface for all standard digital I/Os. Each port has the same software interfaces for the operation as General Purpose I/O and it further provides the connectivity to the on-chip peripherals and the control for the pad characteristics. :

The GPIO provides following features:

- Bidirectional port features (P0, P1)
  - P0/P1: Configurable pin direction
  - P0/P1: Configurable pull-up/pull-down devices
  - P0/P1: Configurable open drain mode
  - P0/P1: Configurable drive strength
  - P0/P1: Configurable slew rate
  - P0/P1: Transfer of data through digital inputs and outputs (general purpose I/O)
  - P0/P1: Possible readback of pin status when GPIO is configured as output (short detection)
  - P0/P1: Alternate input/output for on-chip peripherals
  - P0/P1: up to seven alternate output connections from peripherals selectable. The three configuration bits per GPIO are located in the same register
  - P0/P1: separate input and output registers, which allows to evaluate the input while the output is active (plausibility check)
  - P0/P1: dedicated output modification registers (enabling set, clear, toggle functionality) to avoid read-modify-write operations
  - P0/P1: default configuration during bootup is input and floating (no pull-up/pull-down)
- Analog port features (P2)
  - P2: Configurable pull-up/pull-down devices
  - P2: Transfer of data through digital inputs
  - P2: Alternate inputs for on-chip peripherals
  - P2: Disabling of digital input stage on shared analog input ports
- Wake-up feature
  - Configurable wake-up from stop mode via GPIO (rising edge only, falling edge only, both edges), e.g. for wake-up on a sensor signal
  - In total 6 port pins can be configured for wake-up, freely selectable from P0/P1/P2
  - No lost wake-up, independent from the timing relationship between the wake-up event and the stop-entry command

13.2 Block diagram

Port 0 and Port 1

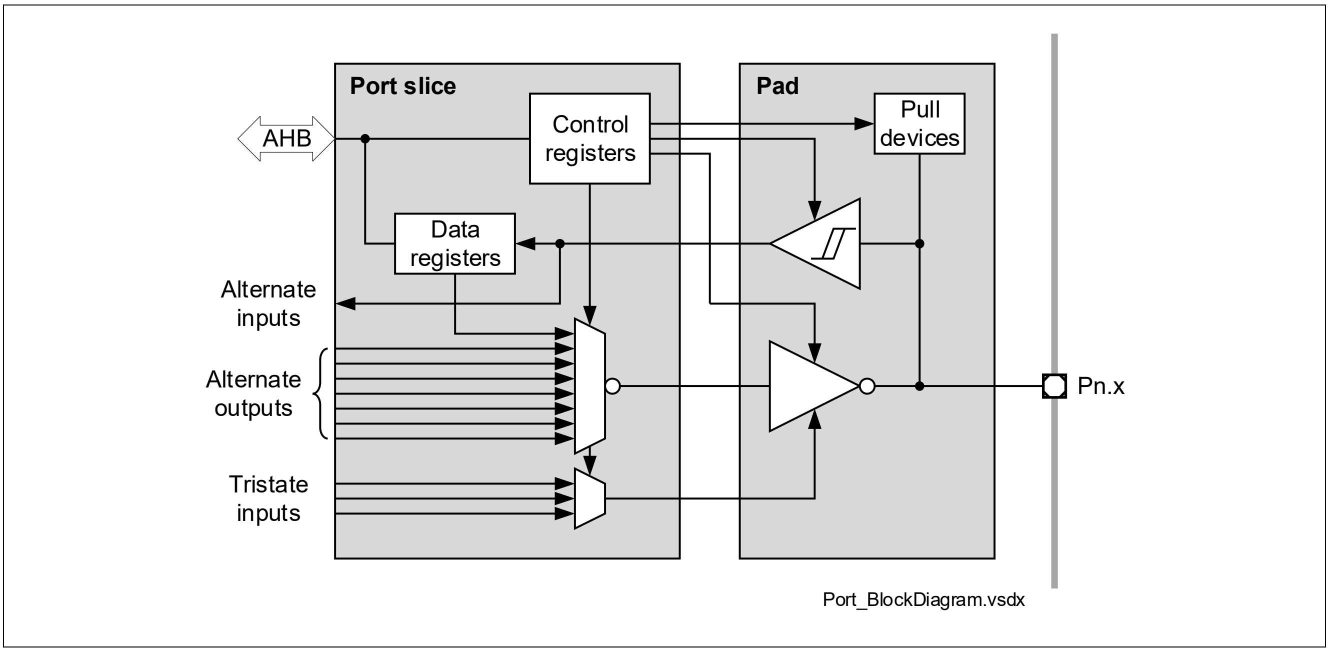


Figure 20 General structure of bidirectional port

Port 2

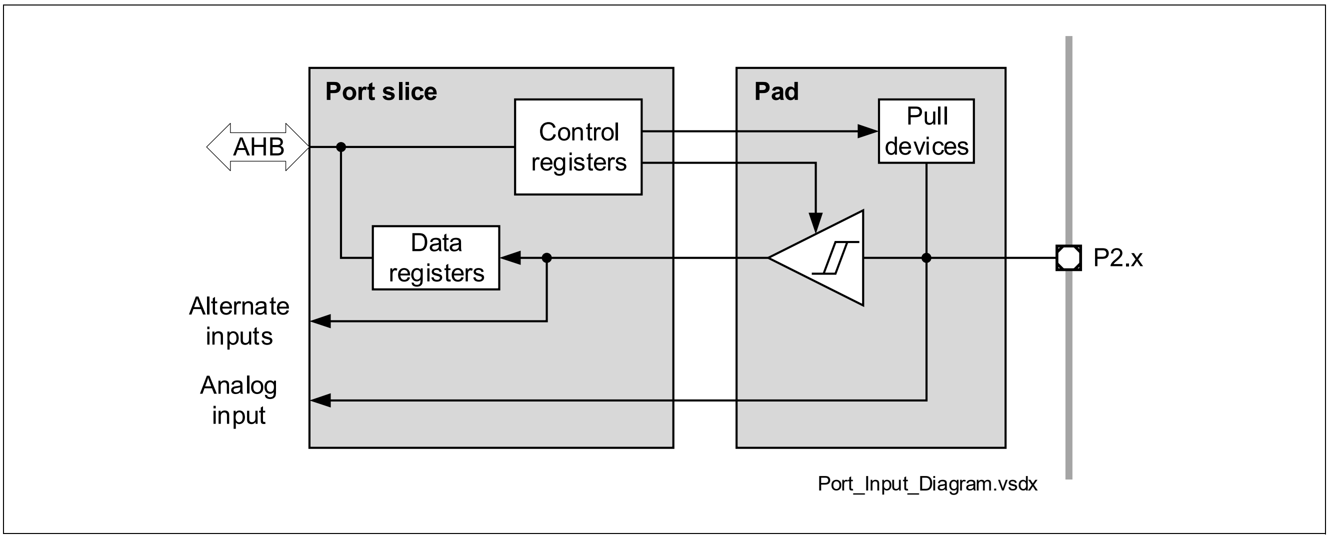


Figure 21 General structure of input port

13.3 Electrical characteristics GPIO

13.3.1 Description of keep and force current

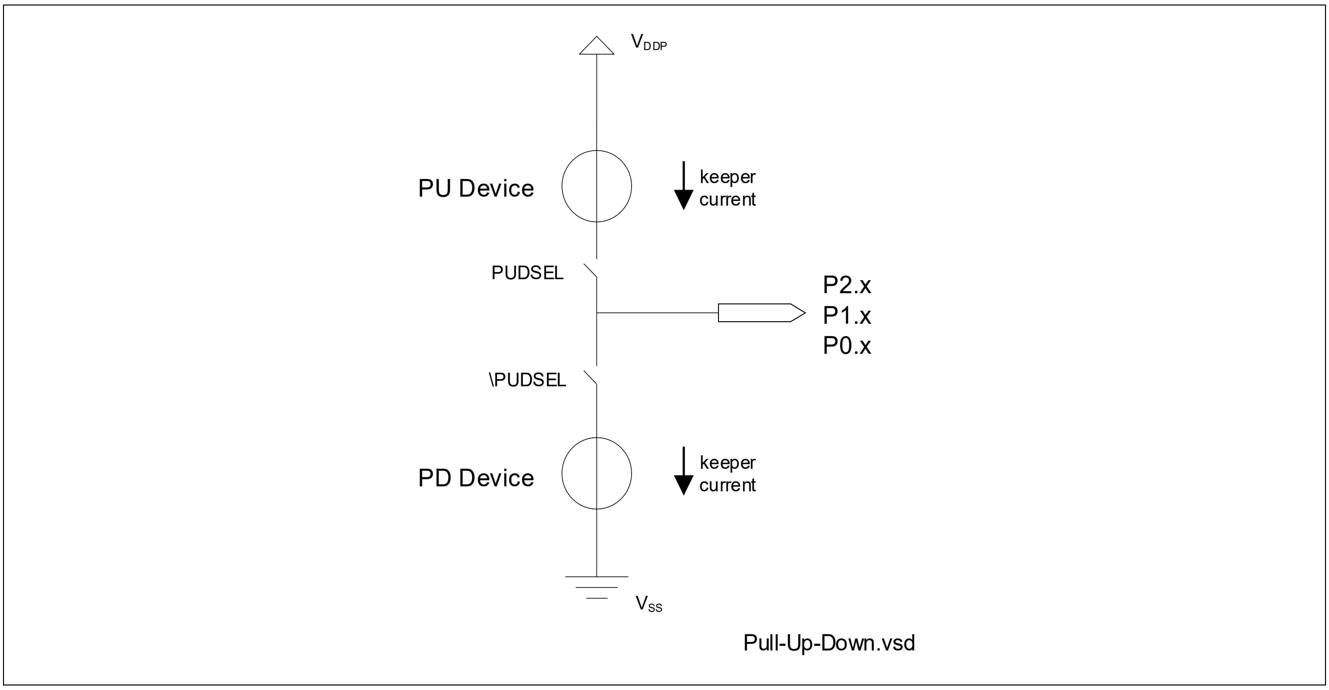


Figure 22 **Pull-up/pull-down device**

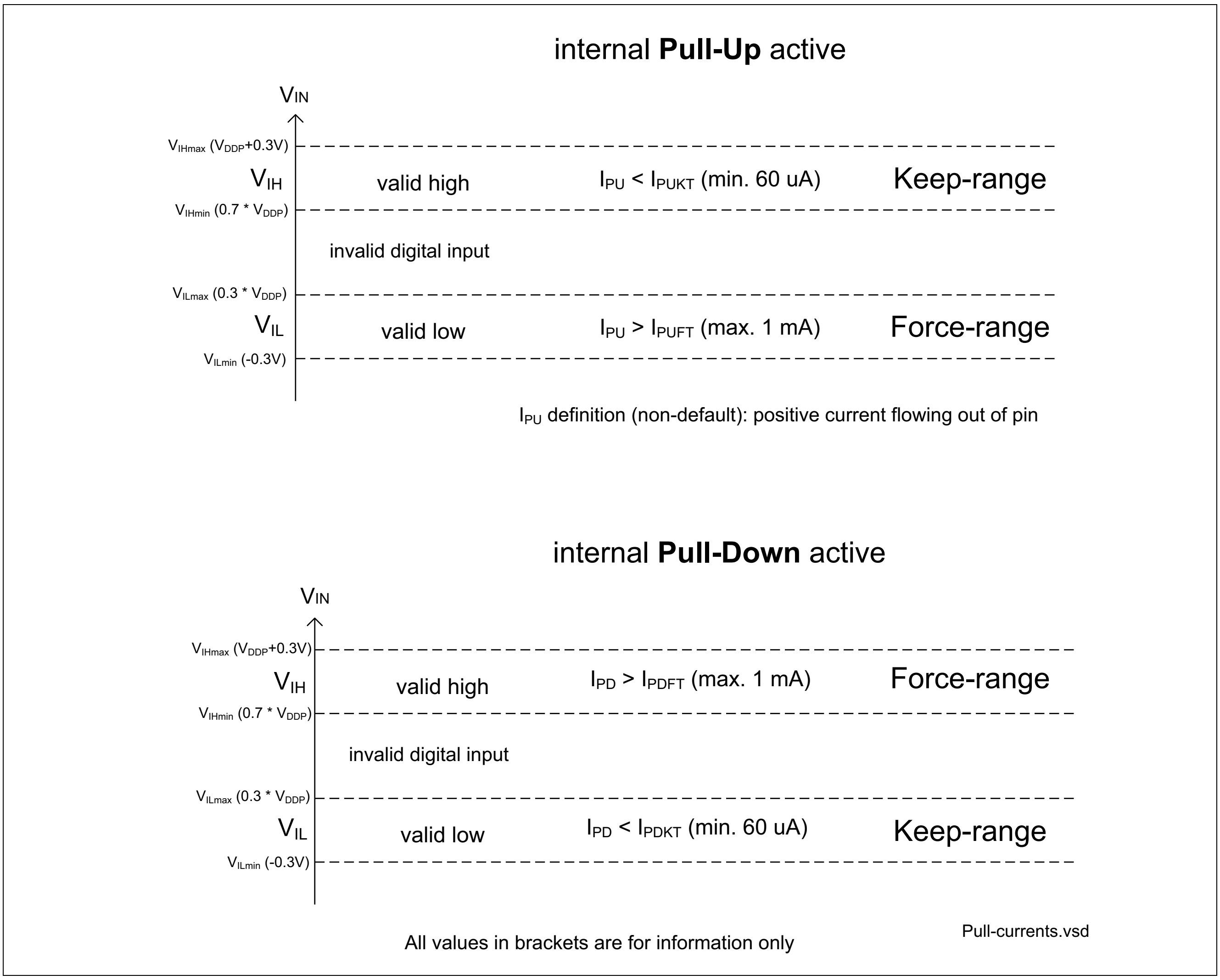


Figure 23 Pull currents, Keep and Force Current

13.3.2 Port 0, Port 1, TMS and Reset DC characteristics

Note: Operating Conditions apply.
Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Table 44 DC Characteristics Port0, Port1, TMS, Reset

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage	V_{IL}	-0.3	-	0.3 * V_{DDP}	V	2.55V≤V_{DDP}≤5.5V	P_GPIO_01_01
Input high voltage	V_{IH}	0.7 * V_{DDP}	-	V_{DDP} + 0.3	V	2.55V≤V_{DDP}≤5.5V	P_GPIO_01_02
Input Hysteresis	Hys	0.11 * V_{DDP}	-	-	V	[1] 4.5V≤V_{DDP}≤5.5V; Series Resistance=0Ω	P_GPIO_01_03
Input Hysteresis	Hys_{ext}	0.04 * V_{DDP}	-	-	V	[1] 2.55V≤V_{DDP}<4.5V; Series Resistance=0Ω	P_GPIO_01_04
Input leakage current	I_{OZ2}	-5	-	+5	µA	T_j≤85°C; 0V<V_{IN}<V_{DDP}	P_GPIO_01_05
Input leakage current	I_{OZ2ext}	-22	-	+22	µA	0V<V_{IN}<V_{DDP}	P_GPIO_01_06
Pull-up keep threshold	I_{PUKT}	60	-	-	µA	[2] [3] 4.5V≤V_{DDP}≤5.5V; V_{IN}=V_{IHmin}	P_GPIO_01_07
Pull-up force threshold	I_{PUFT}	-	-	1	mA	[2] [3] 4.5V≤V_{DDP}≤5.5V; V_{IN}=V_{ILmax}	P_GPIO_01_08
Pull-down keep threshold	I_{PDKT}	60	-	-	µA	[2] 4.5V≤V_{DDP}≤5.5V; V_{IN}=V_{ILmax}	P_GPIO_01_09
Pull-down force threshold	I_{PDFT}	-	-	1	mA	[2] 4.5V≤V_{DDP}≤5.5V; V_{IN}=V_{IHmin}	P_GPIO_01_10
Pin capacitance	C_{IO}	-	-	10	pF	[1]	P_GPIO_01_11
Output low voltage (max. current)	$V_{OL\_max\_cur}$	-	-	1.0	V	[4] [5] I_{OL}≤I_{OLmax} ; 2.55V≤V_{DDP}≤5.5V	P_GPIO_01_13
Output low voltage (nom. current)	$V_{OL\_nom\_cur}$	-	-	0.4	V	[4] [5] I_{OL}≤I_{OLnom} ; 2.55V≤V_{DDP}≤5.5V	P_GPIO_01_14
Output high voltage (max. current)	$V_{OH\_max\_cur}$	V_{DDP} - 1.0	-	-	V	[4] [5] [6] I_{OH}≤I_{OHmax} ; 2.55V≤V_{DDP}≤5.5V	P_GPIO_01_15
Output high voltage (nom. current)	$V_{OH\_nom\_cur}$	V_{DDP} - 0.4	-	-	V	[4] [5] [6] I_{OH}≤I_{OHnom} ; 2.55V≤V_{DDP}≤5.5V	P_GPIO_01_16

Table 44 DC Characteristics Port0, Port1, TMS, Reset (cont'd)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Slope (strong driver, sharp edge), rise / fall time	$t_{\text{slope,sharp}}$	-	-	15	ns	[7] C_L≤100pF	P_GPIO_01_17
		-	-	5	ns	[7] C_L≤20pF	P_GPIO_01_18
Output Slope (medium driver), rise / fall time	$t_{\text{slope,medium}}$	-	-	50	ns	[7] C_L≤100pF	P_GPIO_01_19
		-	-	12	ns	[7] C_L≤20pF	P_GPIO_01_20

1) Not subject to production test, specified by design

2) Keep current: Limit the current through this pin below the threshold so that the enabled pull device can keep the pin level.
Force current: Drive at least the threshold current through this pin to override the pin level driven by the enabled pull device.
See also figure "Pull currents, Keep and Force Current".
These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.

3) I_{PU} definition (non-default): positive current flowing out of pin

4) The maximum deliverable output current of a port driver depends on the selected output driver mode. The limit for pin groups must be respected.

5) I_{OLnom}, I_{OLmax}, I_{OHnom}, I_{OHmax}: see Table "Current Limits for Port Output Drivers"

6) I_{OH} definition (non-default): positive current flowing out of pin

7) 20% / 80% of V_{DDP}

Table 45 Current Limits for Port Output Drivers

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Current, Strong Driver	I_{OLHs5}	-	1.6	5	mA	[1] [2] V_{DDP}≥4.5V	P_GPIO_02_01
Output Current, Medium Driver	I_{OLHm5}	-	1.0	3	mA	[1] [2] V_{DDP}≥4.5V	P_GPIO_02_02
Output Current, Weak Driver	I_{OLHw5}	-	0.25	0.5	mA	[1] [2] V_{DDP}≥4.5V	P_GPIO_02_03
Output Current, Strong Driver	I_{OLHs3}	-	1.0	3	mA	[1] [2] 2.55V≤V_{DDP}<4.5V	P_GPIO_02_04
Output Current, Medium Driver	I_{OLHm3}	-	0.8	1.8	mA	[1] [2] 2.55V≤V_{DDP}<4.5V	P_GPIO_02_05
Output Current, Weak Driver	I_{OLHw3}	-	0.15	0.3	mA	[1] [2] 2.55V≤V_{DDP}<4.5V	P_GPIO_02_06

1) Typ. values: Nominal Output Current (I_{OLnom}, I_{OHnom}).
Max. values: Maximum Output Current (I_{OLmax}, I_{OHmax}).
Values are valid for both Lowside current and Highside current.

2) I_{OH} definition (non-default): positive current flowing out of pin

13.3.3 Port 2 DC characteristics

Note: Operating Conditions apply.
Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Table 46 DC Characteristics Port 2

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	**Symbol**	**Values**			**Unit**	**Note or Test Condition**	**Number**
		Min.	**Typ.**	**Max.**			
Input low voltage	V_{IL_P2}	-0.3	-	0.3 * V_{DDP}	V	2.55V≤V_{DDP}≤5.5V	P_GPIO_03_01
Input high voltage	V_{IH_P2}	0.7 * V_{DDP}	-	V_{DDP} + 0.3	V	2.55V≤V_{DDP}≤5.5V	P_GPIO_03_02
Input Hysteresis	Hys_{P2}	0.11 * V_{DDP}	-	-	V	[1] 4.5V≤V_{DDP}≤5.5V; Series Resistance=0Ω	P_GPIO_03_03
Input Hysteresis	Hys_{P2ext}	0.04 * V_{DDP}	-	-	V	[1] 2.55V≤V_{DDP}<4.5V; Series Resistance=0Ω	P_GPIO_03_04
Input leakage current	I_{OZ1_P2}	-400	-	+400	nA	[2] T_j≤85°C; 0V<V_{IN}<5.1V	P_GPIO_03_05
Input leakage current	I_{OZ1_P2ext}	-1	-	+1	µA	[2] 0V<V_{IN}<5.1V	P_GPIO_03_06
Pull-up keep threshold	I_{PUKT_P2}	60	-	-	µA	[3] [4] 4.5V≤V_{DDP}≤5.5V; V_{IN}=V_{IHmin}	P_GPIO_03_07
Pull-up force threshold	I_{PUFT_P2}	-	-	1	mA	[3] [4] 4.5V≤V_{DDP}≤5.5V; V_{IN}=V_{ILmax}	P_GPIO_03_08
Pull-down keep threshold	I_{PDKT_P2}	60	-	-	µA	[3] 4.5V≤V_{DDP}≤5.5V; V_{IN}=V_{ILmax}	P_GPIO_03_09
Pull-down force threshold	I_{PDFT_P2}	-	-	1	mA	[3] 4.5V≤V_{DDP}≤5.5V; V_{IN}=V_{IHmin}	P_GPIO_03_10
Pin capacitance (digital inputs/outputs)	C_{IO_P2}	-	-	10	pF	[1]	P_GPIO_03_11

1) Not subject to production test, specified by design
2) An additional error current will flow if an overload current flows through an adjacent pin.
3) Keep current: Limit the current through this pin below the threshold so that the enabled pull device can keep the pin level.
Force current: Drive at least the threshold current through this pin to override the pin level driven by the enabled pull device.
See also figure "Pull currents, Keep and Force Current".
4) I_{PU} definition (non-default): positive current flowing out of pin

14 High-Voltage Monitor Input (MON)

14.1 Features overview

The High-Voltage Monitor Input (MON) is dedicated to monitor external voltage levels above or below the threshold V_{MONth}. Each MONx input can further be used to create a wake-up event by detecting a level change while crossing the threshold. This applies to any system operation mode, especially for the power-down modes. Furthermore each MONx input can be sampled by the ADC1 as an analog input. It can also be used as a high-voltage PWM input signal for Timer21.

The MON provides following features:

- High-voltage inputs with threshold voltage 3 V (typ.)
- Wake-up capability for system Stop mode and system Sleep mode
- Edge sensitive wake-up feature configurable for transitions from low to high, high to low or both directions
- MON input level status (high/low) can be read in Active mode
- MON inputs can also be evaluated with ADC1 in Active mode to sense high-voltage signals, using adjustable threshold values for interrupt generation
- Selectable pull-up and pull-down current sources available
- MON inputs can be selected as inputs for Timer21 to evaluate high-voltage PWM input signals
- MON inputs can be used for edge detection (interrupt generation for transitions from low to high, high to low or both directions)

14.2 Block diagram

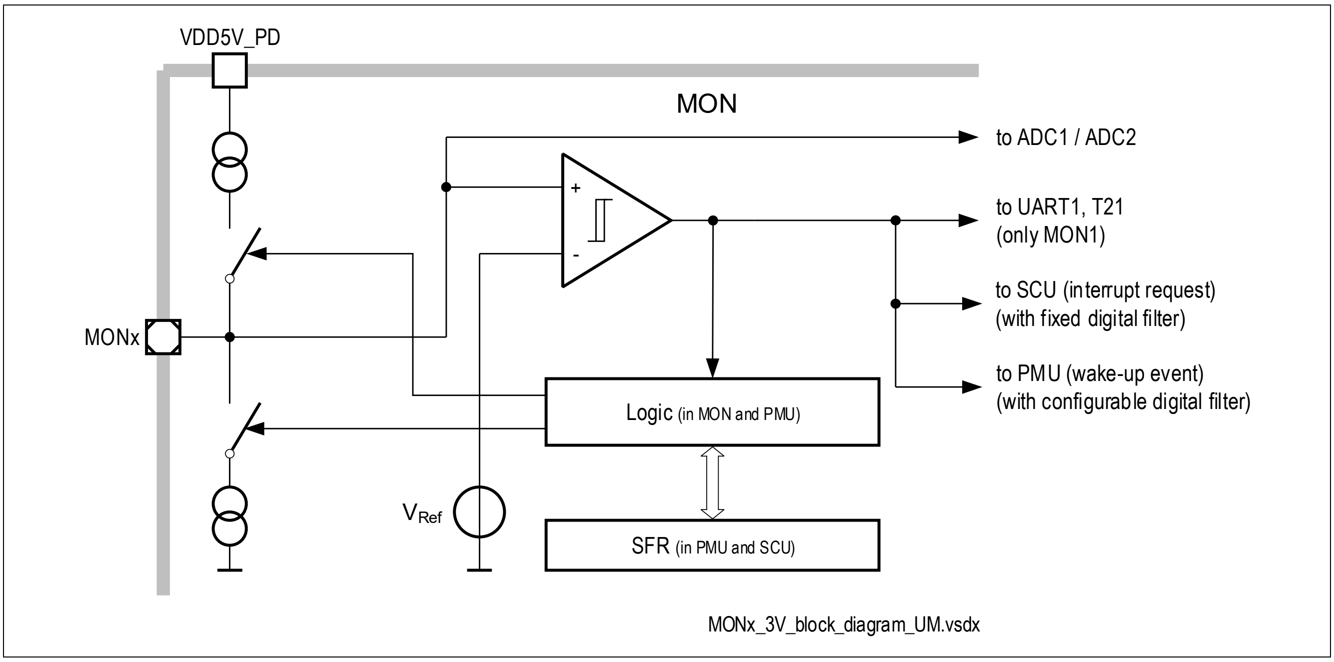


Figure 24 Block diagram MON

14.3 Electrical characteristics MON

14.3.1 MON characteristics

Table 47 Electrical Characteristics Monitoring Input

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Wake-up/monitoring threshold voltage	V_{MONth}	2	3	3.8	V	without external serial resistor R_s (with R_s:dV = $I_{PD/PU}$* R_s);	P_MON_02_01
Threshold hysteresis	$V_{MONth,hys}$	0.1	-	0.7	V	in all modes; without external serial resistor R_s (with R_s:dV = $I_{PD/PU}$* R_s);	P_MON_02_02
Pull-up current	$I_{PU, MON}$	-20	-10	-3	µA	V_{MON_IN}=3.8V	P_MON_02_03
Pull-down current	$I_{PD, MON}$	3	10	20	µA	V_{MON_IN}=2V	P_MON_02_04
Input leakage current	$I_{LK,MON}$	-2	-	2	µA	[1] 0V<V_{MON_IN}<40V	P_MON_02_05

1) Valid for enabled module. Pull-up and pull down current functionality disabled; ADC1 off.

15 Analog Reference Voltage Generation (ARVG)

15.1 Features overview

The Analog Reference Voltage Generation module (ARVG) is responsible for the generation of reference voltages that can be used by the various analog peripherals in the device.

The ARVG provides following features:

- VREF1V2 internal reference voltage generation (V_{REF1V2}, 1.211 V typ.) for ADC2 and the NVM
- VREF1V2 is monitored by ADC1
- VAREF reference voltage generation (V_{REF5V}, 5 V typ.) for ADC1, CSA, CSC and SDADC; VAREF has a pin and needs a buffer cap to VAGND (see $C_{VAREF)}$
- VAREF has an overcurrent (undervoltage) monitor (VAREF_OC)
- VAREF has an overvoltage monitor within the PMU (VAREF_OV), for more details please refer to the **Power Management Unit (PMU)** chapter

15.2 Block diagram

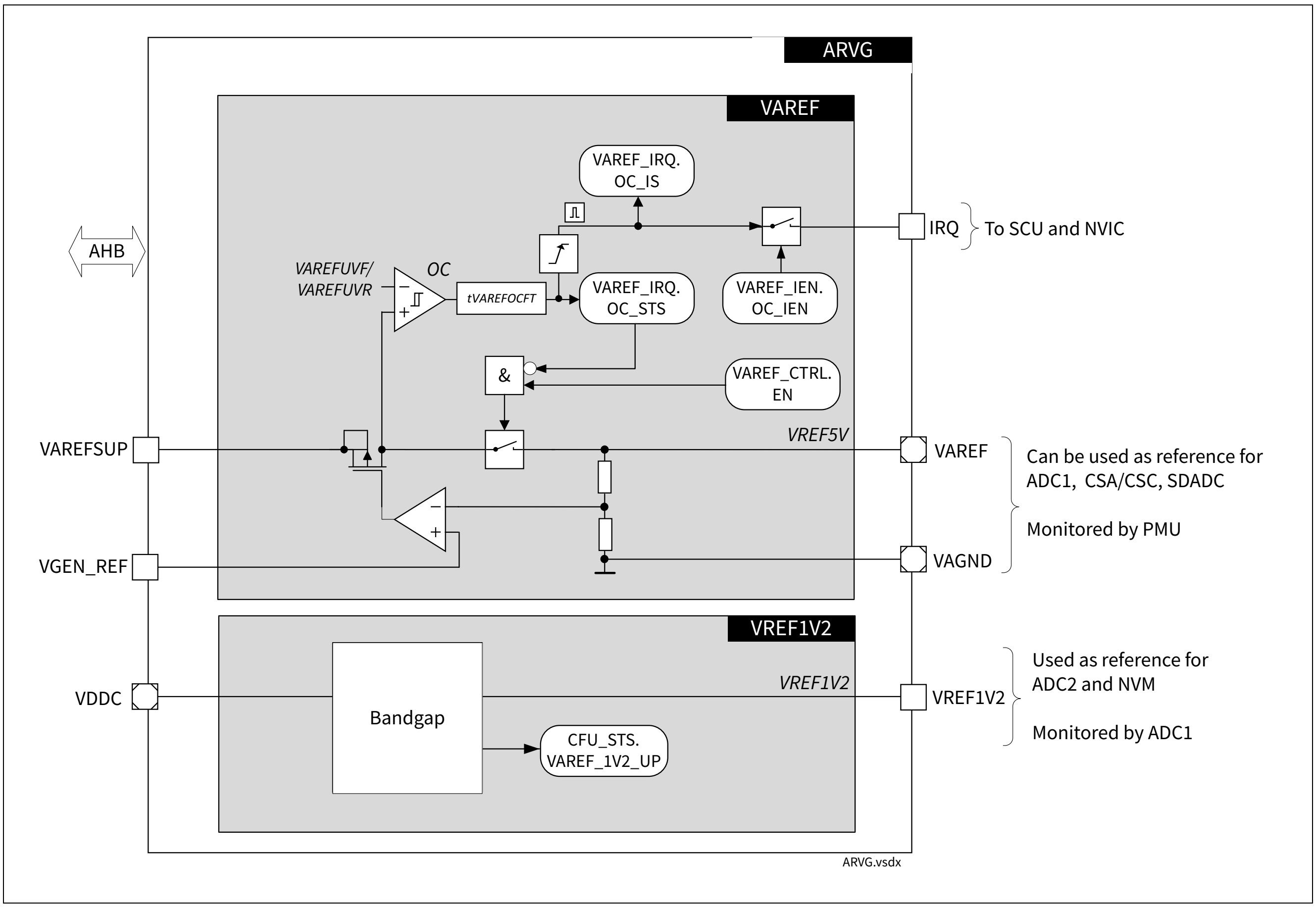


Figure 25 Block diagram ARVG

15.3 Electrical characteristics ARVG

15.3.1 VREF1V2 DC characteristics

Table 48 VREF1V2 DC Specification

V_S = 3 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reference output voltage	V_{REF1V2}	1.188	1.211	1.22	V	all parameters within specification limits	P_ARVG_02_01
Temperature drift	ΔV_{REF1V2}	0	-	1	%	[1] [2]	P_ARVG_02_02

[1] $\Delta V_{REF1V2} = (V_{REF1V2,max} - V_{REF1V2,min}) / V_{REF1V2,min}$ where $V_{REF1V2,min}$ is minimum V_{REF1V2} over temperature range and $V_{REF1V2,max}$ is maximum V_{REF1V2} over temperature range

[2] Not subject to production test, specified by design

15.3.2 VREF5 DC characteristics

Table 49 VREF5 DC Specification

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reference output voltage	V_{REF5V}	4.9	5	5.1	V	all parameters within specification limits	P_ARVG_03_01
Temperature drift	ΔV_{REF5V}	0	-	1	%	[1] [2]	P_ARVG_03_08
Power-up time	t_{WAKE}	50	-	200	µs	VREF5V_ENABLE to 99.9% of the final value; C_{ext}=100nF	P_ARVG_03_02
VAREF required buffer capacitance	C_{VAREF}	0.1	-	1	µF	[2] the specified capacitor value is a value including tolerances; ESR<100mOhm	P_ARVG_03_03
VAREF undervoltage (overcurrent) threshold falling	$V_{AREFUVF}$	2.33	2.48	2.85	V		P_ARVG_03_04
VAREF undervoltage (overcurrent) threshold rising	$V_{AREFUVR}$	3.44	3.74	4	V	[2]	P_ARVG_03_05
VAREF output current	I_{VAREF}	0	-	20	µA	[2]	P_ARVG_03_06
VAREF OC filter time	$t_{VAREFOCFT}$	3.6	4	4.4	µs	[2]	P_ARVG_03_07

1) $\Delta V_{REF5V} = (V_{REF5V,max} - V_{REF5V,min}) / V_{REF5V,min}$ where $V_{REF5V,min}$ is minimum V_{REF5V} over temperature range and $V_{REF5V,max}$ is maximum V_{REF5V} over temperature range

2) Not subject to production test, specified by design

16 Analog Digital Converter 1 (ADC1)

16.1 Features overview

The ADC1 is a successive approximation analog to digital converter which can be used for analog signal measurement especially optimized for BLDC motor control. It has a deterministic behavior regarding to the sample event and conversion timing, even for a sequence of conversions. The ADC1 operates greatly autonomous in background avoiding real-time critical interaction by the CPU or DMA.

The ADC1 provides following features:

- A/D kernel performance:
  - 12-bit resolution for all analog inputs
  - High accuracy of typ. 0.5% of the input range (MV_{ACC}, HV_{ACC1})
  - Fast sampling time ($tsamp_{MV}$, $tsamp_{HV}$, $tsamp_{SHx}$)
  - Fast total conversion time (typ. 800 ns for MV/HV inputs and 1600 ns for SHx inputs)
- Analog inputs ANx:
  - Up to 11 middle voltage inputs (range MVRNG)
  - 8 factory calibrated high voltage inputs (range HVRNG1)
  - Referenced to VAREF/VAGND via internal VAREF or VDDEXT voltage regulators
- Digital channels with channel control and result generation:
  - Each analog input can be freely assigned to one or more out of 20 possible digital channels
  - Each digital channel has its own result register with a result event (IRQ capable)
  - One out of 4 conversion classes can be assigned to a digital channel
  - Up to 4 digital comparators with 8-bit upper and lower thresholds can monitor a channel result and generate a compare event (IRQ and/or interconnect signal)
  - Up to 4 first order IIR filter s with programmable characteristics can be assigned to a channel result
  - Programmable repeat feature for each channel
- Trigger and gating control:
  - For deterministic control of complex conversion sequences with respect to time-accuracy and time-equidistancy
  - 36 trigger inputs can be selected for hardware or software-based start event of a conversion sequence
  - 16 gating inputs can be selected for hardware or software-based gating of a trigger event
- Sequencer:
  - Allows to build complex and variable conversion schemes
  - Up to 4 independent sequences with up to 4 digital channels can be freely assembled
  - Hardware or software-based trigger of a sequence with deterministic end of sequence event (IRQ capable)
  - Possible trigger features: self-trigger or next-sequence-trigger (round robin capable)
  - Shadow mechanism for data coherency when updating the sequencer configuration on-the-fly
- Conversion class control:
  - Programmable sample time adjustment to adapt to the analog input characteristic
  - Programmable noise reduction feature (oversampling, averaging, sample point adjust)
  - Programmable broken wire detection feature for external sensors

  - Programmable calibration feature to compensate drift and temperature effects
- Interrupt and DMA:
  - The ADC1 events can be routed to 4 interrupt node pointers (with 4 IRQ lines)
  - ADC1 events can be mapped to 8 DMA channels

16.2 Block diagram

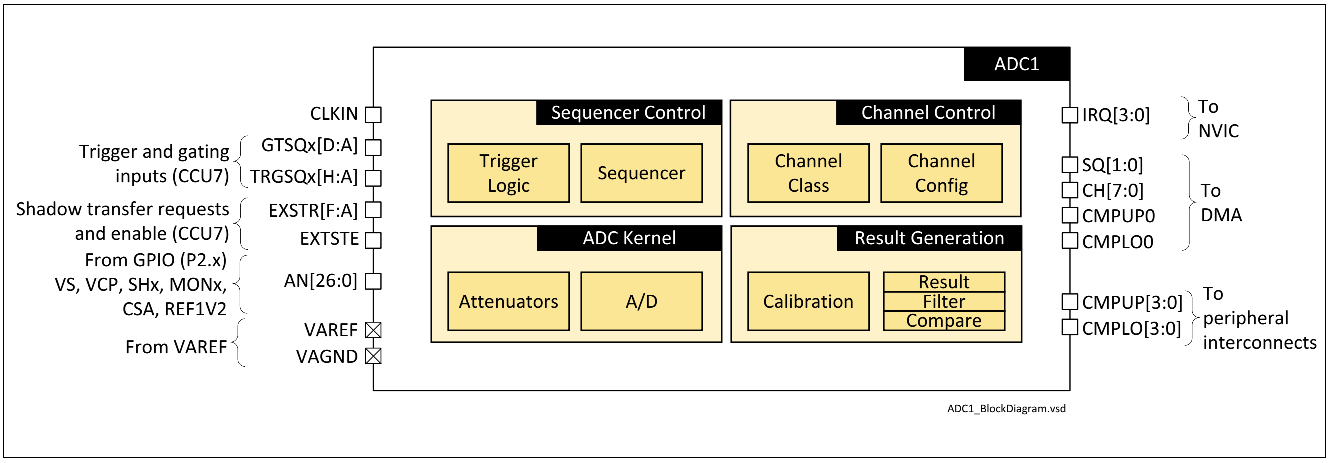


Figure 26 **Block diagram ADC1**

16.3 Electrical characteristics ADC1

16.3.1 A/D converter characteristics ADC1

Table 50 A/D converter ADC1, Timing parameters

V_S = 4.2 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reference ground	*VAGND*	-0.05	-	0.05	V	@VAGND pin; tested with VAREF=VREF5V, VAGND = n.c., blocking cap 100nF between VAREF and VAGND	P_ADC1_01_05
Module Clock Frequency	*fadc*	5	-	40	MHz	Internal ADC1 clock derived from module input clock via CLKDIV	P_ADC1_01_36
Sample Time HV input	$tsamp_{HV}$	200	-	-	ns	[1] STC has to be programmed accordingly	P_ADC1_01_38
Sample Time SHx input	$tsamp_{SHx}$	1000	-	-	ns	[1] STC has to be programmed accordingly	P_ADC1_01_44
Sample Time MV input	$tsamp_{MV}$	200	-	-	ns	[1] STC has to be programmed accordingly	P_ADC1_01_40

1) Not subject to production test, specified by design

Table 51 A/D converter ADC1, Performance parameters

V_S = 4.2 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), LSB = VAREF/4096

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Integral Nonlinearity	*INLE*	-4	-	4	LSB		P_ADC1_01_18
Differential Nonlinearity	*DNLE*	-1	-	2	LSB	[1] No two consecutive missing codes	P_ADC1_01_20
Total Unadjusted Error for HV inputs	TUE_{HV}	-7	-	7	LSB	[2] [1]	P_ADC1_01_30
Total Unadjusted Error for MV inputs	TUE_{MV}	-6	-	6	LSB	[2] [1]	P_ADC1_01_28
RMS Noise 1	RMS_1	-	1.5	2	LSB	[1]	P_ADC1_01_32

Table 51 A/D converter ADC1, Performance parameters (cont'd)

V_S = 4.2 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), LSB = VAREF/4096

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
RMS Noise 3	RMS_3	-	-	1.4	LSB	[1] With averaging of 4 oversampling conversions	P_ADC1_01_34
Negative overload coupling factor	*KOVAN*	-	-	0.00015		[3] [4] [5] [1]	P_ADC1_01_08
Positive overload coupling factor	*KOVAP*	-	-	0.00015		[3] [4] [5] [1]	P_ADC1_01_09
Discharge current for broken wire detection setting 0	*Ibwd*	60	80	100	µA		P_ADC1_01_06
Discharge current for broken wire detection setting 1	*Ibwdh*	480	640	800	µA		P_ADC1_01_07
Analog input resistance	R_{AIN}	-	-	34	kΩ	[1] This is the internal resistive path from ANx pad via mux to the cap field	P_ADC1_01_12
Switched capacitance at ANx	C_{AIN}	-	-	660	fF	[1] This is the capacitance which must be charged by the analog source within the minimum sampling time	P_ADC1_01_13
Analog reference input resistance	R_{AREF}	-	-	7	kΩ	[1] This is the internal resistive path from VAREF pad to cap field	P_ADC1_01_15
Switched capacitance at VAREF	C_{AREF}	-	-	330	fF	[1] This is the capacitance which must be charged by VAREF source with the first successive approximation cycle	P_ADC1_01_17
Power Supply Rejection Ratio for High Voltage Inputs	$PSSR_{HV}$	25	-	-	dB	[1] @VDDP with 3 kHz, 100 mV peak-to peak ripple	P_ADC1_01_42
Power Supply Rejection Ratio for Mid Voltage Inputs	$PSSR_{MV}$	5	-	-	dB	[1] @VDDP with 3 kHz, 100 mV peak-to peak ripple	P_ADC1_01_43

1) Not subject to production test, specified by design

2) TUE = (INL × GE) + OE, without channel calibration.

3) The overload coupling factor KOVAN/KOVAP (K) defines the worst case relation of an overload condition (Iov) at one pin to the resulting leakage current (Ileaktot) into an adjacent pin: Ileaktot = ±K × |Iov| + Ioz1. Thus the overload condition can cause an an additional error voltage at an adjacent analog input pin.
4) Overload current is allowed in following operation modes: unpowered, active and sleep mode.
5) Overload conditions occur if the standard operating conditions are exceeded, i.e. the input voltage V_{in} at the pin exceeds the specified range: V_{in} > VDDP + 0.3 V (Iov > 0) or V_{in} < -0.3 V (Iov < 0).

16.3.2 Analog inputs characteristics

Table 52 HV inputs with attenuator type 0 (ATT_TYP0)

V_S = 5.5 V to 40 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Nominal HV input voltage range 0	HV_{RNG0}	0	-	25.09	V	not calibrated	P_ADC1_02_01
Accuracy of measurement with ATT_{TYP0}	HV_{ACC0}	-250	-	250	mV	[1] not calibrated	P_ADC1_02_02

[1] Not subject to production test; referenced to V_{in}.

Table 53 HV inputs with attenuator type 1 (ATT_TYP1)

V_S = 5.5 V to 40 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Nominal HV input voltage range 1	HV_{RNG1}	0	-	35.555	V		P_ADC1_03_01
Accuracy of measurement with ATT_{TYP1} at input voltage range 1	HV_{ACC1_1}	-125	-	125	mV	[1] with calibration enabled (CALENi=1); $0V<V_{IN}\leq 10.6V$	P_ADC1_03_03
Accuracy of measurement with ATT_{TYP1} at input voltage range 2	HV_{ACC1_2}	-150	-	150	mV	[1] with calibration enabled (CALENi=1); $10.6V<V_{IN}\leq 17.7V$	P_ADC1_03_04
Accuracy of measurement with ATT_{TYP1} at input voltage range 3	HV_{ACC1_3}	-235	-	235	mV	[1] with calibration enabled (CALENi=1); $17.7V<V_{IN}\leq 35.5V$	P_ADC1_03_02

[1] Five points of transfer curve for each analog input; @hot and @cold temperature; each point averaged over 16 measurements.

Table 54 MV inputs with attenuator type 2 (ATT_TYP2)

V_S = 5.5 V to 40 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Nominal MV input voltage range	MV_{RNG}	0	-	5	V	with calibration enabled (CALENi=1); in case VAREF is externally supplied the condition VAREF < *VDDP* + 0.3 V must be met	P_ADC1_04_01
Accuracy of measurement with ATT_{TYP2}	MV_{ACC}	-35	-	35	mV	[1] with calibration enabled (CALENi=1)	P_ADC1_04_02
Accuracy of measurement with ATT_{TYP2}	MV_{ACC_CSA}	-60	-	60	mV	for CSA (ADC1 channel 18); *G*=40 ; CTRL2.OFFS_SEL<1:0 >=00_B	P_ADC1_04_03
		-90	-	90	mV	for CSA (ADC1 channel 18)	P_ADC1_04_04

---

1) Five points of transfer curve for each analog input; @hot and @cold temperature; each point averaged over 16 measurements.

17 Monitoring Analog Digital Converter 2 (ADC2)

17.1 Features overview

The ADC2 is a successive approximation analog to digital converter which is used for diagnosis of internal system voltages. The ADC2 has a pre-configured sequence of conversions with a deterministic timing. It runs fully autonomous in background, provides the digital results and generates events for interrupts and interconnects.

The ADC2 has following features:

- A/D kernel performance:
  - 10-bit resolution for all analog inputs
  - Wide input range for middle and high voltage inputs from typ. 5 V to 50 V (MV_{RNG}, $HV_{RNG0/1/2/3}$)
  - High accuracy of typ. 1% of the input range (MV_{ACC}, $HV_{ACC0/1/2/3}$)
  - Fast sampling time ($tsamp_{MV}$, $tsamp_{HV}$)
  - Fast total conversion time (typ. 1 µs for MV and typ. 2 µs for HV inputs)
- Analog inputs ANx:
  - 8 factory calibrated middle voltage inputs (range MV_{RNG})
  - Up to 7 factory calibrated high voltage inputs (ranges $HV_{RNG0/1/2/3}$)
  - Referenced to internally generated VREF1V2 reference voltage (see the **Analog Reference Voltage Generation (ARVG)** chapter)
- Digital channels with channel control and result generation:
  - Each analog input is assigned to one digital channel and has a separate result register
  - 6 digital channels are pre-set for monitoring and protection function for BDRV and CANTRX (NMI capable)
  - 2 freely selectable digital comparators with programmable upper and lower thresholds (8-bit) for user defined monitoring (IRQ capable)
  - 2 freely selectable first order IIR filters with programmable characteristics for result post-processing
  - Results can be read at any time by user software
- Sequencer:
  - One fixed conversion sequence is pre-programmed and runs in a round-robin scheme autonomously in background
- Interrupt and DMA:
  - The ADC2 events can generate a NMI
  - The ADC2 events can be mapped to 2 interrupt node pointers (with 2 IRQ lines)

17.2 Block diagram

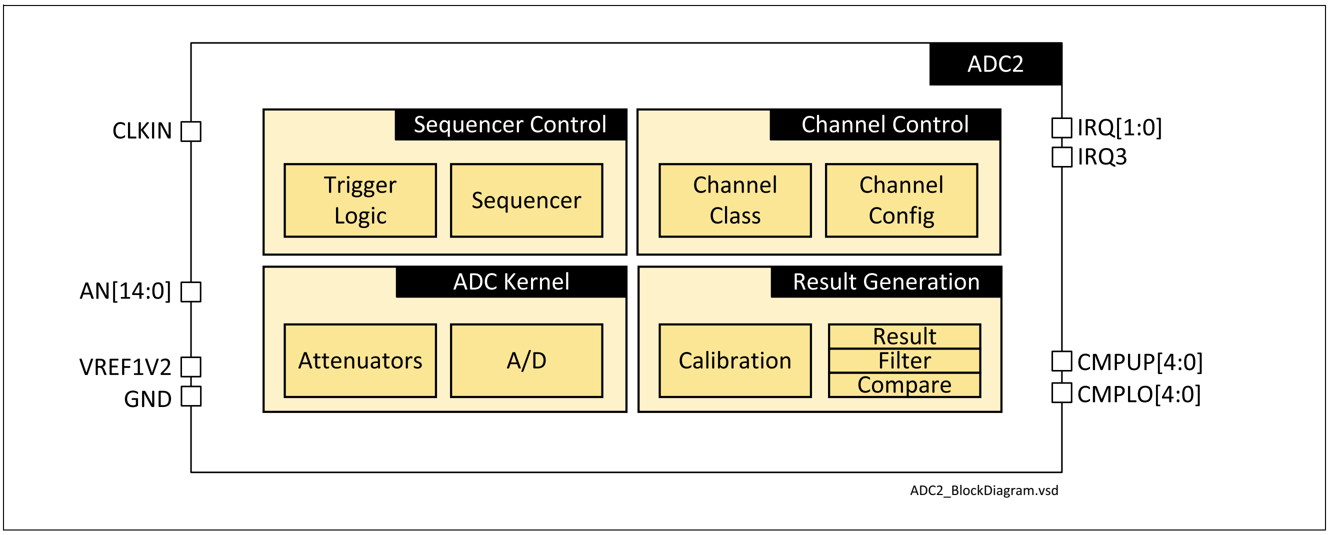


Figure 27 Block diagram ADC2

17.3 Electrical characteristics ADC2

17.3.1 A/D converter characteristics ADC2

Table 55 A/D Converter - Timing and AC specification

V_S = 3 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Analog clock frequency	f_{ADC2}	5	-	40	MHz	Internal ADC2 clock derived from module input clock via CLKDIV	P_ADC2_02_02
Sampling time for high voltage inputs	$tsamp_{HV}$	1400	-	-	ns		P_ADC2_02_03
Sampling time for medium voltage input	$tsamp_{MV}$	400	-	-	ns		P_ADC2_02_05
RMS noise	*RMS*	0	-	1.8	LSB	[1] [2]	P_ADC2_02_10

1) Design characterization: 5000 samples @ VIN=4.75V; value @ 1 sigma

2) Not subject to production test, specified by design

Table 56 A/D Converter - DC specification

V_S = 3 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Differential nonlinearity	*DNLE*	-0.99	-	2	LSB	no missing codes	P_ADC2_03_01
Integral nonlinearity	*INLE*	-2	-	2	LSB	maximum deviation from linear best fit line	P_ADC2_03_02
Gain error	*GE*	-1.2	-	1.2	%	[1]	P_ADC2_03_03
Offset error	*OE*	-3	-	3	LSB	[2] V_S=13.5V; f_{ADC2}=30MHz	P_ADC2_03_04
Total unadjusted error	*TUE*	-8	-	8	LSB	[2]	P_ADC2_03_05
On resistance of a HV analog input	R_{AON_HV}	4	5.5	7.5	kΩ	[2]	P_ADC2_03_06
Input capacitance of a HV analog input	C_{AIN_HV}	80	180	310	fF	[2]	P_ADC2_03_07

Table 56 A/D Converter - DC specification (cont'd)

V_S = 3 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
On resistance of a MV analog input	R_{AON_MV}	8	13	19	kΩ	[2]	P_ADC2_03_08
Input capacitance of a MV analog input	C_{AIN_MV}	325	435	545	fF	[2]	P_ADC2_03_09

1) After analog input calibration, including temperature drift of GE and VREF1V2; temperature drift of GE and temperature drift of VREF1V2 may compensate each other; GE is relative to the full scale range; the GE at half scale range is only half of the full scale range error

2) Not subject to production test, specified by design

17.3.2 Attenuators characteristics

Table 57 Attenuator type 0 for HV inputs

V_S = 3 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Nominal HV input voltage range 0	HV_{RNG0}	0	-	25.83	V	HV_{RNG0}=VREF1V2(typ)/ ATT_{TYP0}	P_ADC2_04_01
Accuracy of measurement with ATT_{TYP0}	HV_{ACC0}	-220	-	220	mV	[1]	P_ADC2_04_02

1) Five points of transfer curve for each analog input; @hot and @cold temperature; each point averaged over 16 measurements

Table 58 Attenuator type 1 for HV inputs

V_S = 3 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Nominal HV input voltage range 1	HV_{RNG1}	0	-	31.00	V	HV_{RNG1}=VREF1V2(typ)/ ATT_{TYP1}	P_ADC2_05_01
Accuracy of measurement with ATT_{TYP1}	HV_{ACC1}	-250	-	250	mV	[1] V_S≥5.5V	P_ADC2_05_02
		-275	-	275	mV	[1] V_S<5.5V	P_ADC2_05_03

1) Five points of transfer curve for each analog input; @hot and @cold temperature; each point averaged over 16 measurements

Table 59 Attenuator type 2 for HV inputs

V_S = 3 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Nominal HV input voltage range 2	HV_{RNG2}	0	-	51.67	V	HV_{RNG2}=VREF1V2(typ)/ ATT_{TYP2}	P_ADC2_06_01
Accuracy of measurement with ATT_{TYP2}	HV_{ACC2}	-500	-	500	mV	[1]	P_ADC2_06_02
		-450	-	450	mV	[1] T_j≤150°C	P_ADC2_06_03

[1] Five points of transfer curve for each analog input; @hot and @cold temperature; each point averaged over 16 measurements

Table 60 Attenuator type 3 for HV inputs

V_S = 3 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Nominal HV input voltage range 3	HV_{RNG3}	0	-	8.15	V	HV_{RNG3}=VREF1V2(typ)/ ATT_{TYP3}	P_ADC2_07_01
Accuracy of measurement with ATT_{TYP3}	HV_{ACC3}	-100	-	100	mV	[1]	P_ADC2_07_02

[1] Five points of transfer curve for each analog input; @hot and @cold temperature; each point averaged over 16 measurements

Table 61 Attenuator type 4 for MV inputs

V_S = 3 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Nominal MV input voltage range	MV_{RNG}	0	-	5.34	V	MV_{RNG}=VREF1V2(typ)/ ATT_{TYP4}	P_ADC2_08_01
Accuracy of measurement with ACC_{TYP4}	MV_{ACC}	-50	-	50	mV	[1] MV measurements are dependent on VDDP, therefore MV_ACC is valid for VIN < VDDP + 0.2 V	P_ADC2_08_02

[1] Five points of transfer curve for each analog input; @hot and @cold temperature; each point averaged over 16 measurements

18 Current Sense Amplifier (CSA)

18.1 Features overview

The Current Sense Amplifier (CSA) in **Figure 28** can be used to measure near-ground differential voltages via ADC1. Its gain and output offset voltage are digitally programmable through internal control registers.

Linear calibration has to be applied to achieve high gain accuracy, e.g. end-of-line calibration including the shunt resistor.

Figure 28 shows how the current sense amplifier can be used as a low-side current sense amplifier where the motor current is converted to a voltage by means of a shunt resistor R_{SH}. A differential amplifier input is used in order to eliminate measurement errors due to voltage drop across the stray resistance R_{Stray} and differences between the external and internal ground. If the voltage at one or both inputs (CSAP/CSAN) is out of the operating range it has to be taken into account that the input circuit is overloaded and needs a certain specified recovery time.

In general, the external low pass filter should suppress electromagnetic interferences (EMI).

The CSA provides following features:

- The CSA amplifies a near-ground differential input voltage to a single-ended output voltage
- The CSA has programmable gain settings of G = 10, 20, 40, 60
- The CSA output voltage has a programmable offset
- The CSA output voltage can be measured by the ADC1
- The CSA output voltage offset can be measured by the ADC1 independently from the CSA input conditions
- The CSA output voltage offset is derived from the ADC1 reference voltage VAREF

18.2 Block diagram

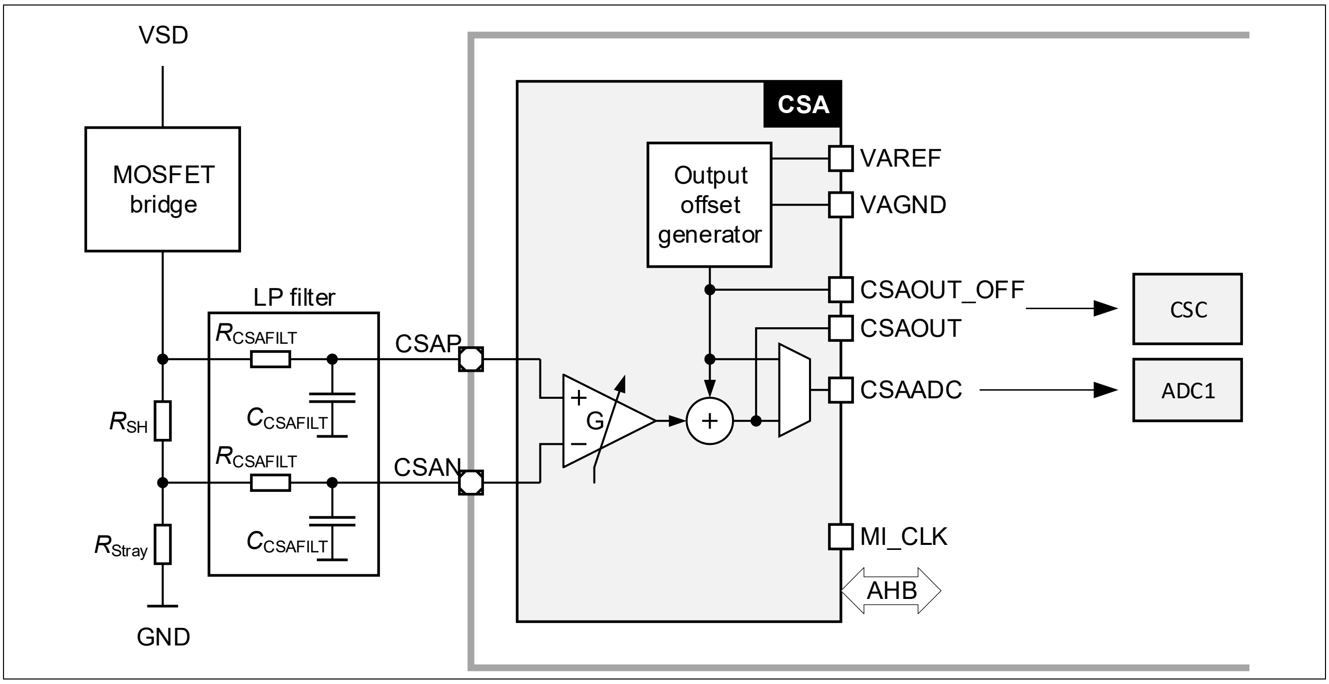


Figure 28 Block diagram CSA

18.3 Electrical characteristics CSA

18.3.1 Description of electrical parameters

Supply range	The CSA is operational for the whole VS supply range
Current consumption	The CSA contributes to the overall device current consumption for the operation modes active, stop, sleep. The overall targets must be achieved.
Differential linear input voltage range	• Difference of input voltages: $V_{CSAIN\_DIFF} = V_{CSAP} - V_{CSAN}$ • Within this range the CSA characteristic is linear • Within this range the CSA errors are inside the specified limits • Symmetry of input voltage range depends on V_{CSAOUT_OFF}
Common mode input voltage range	Voltage range for V_{CSAP} and V_{CSAN}
Single-ended linear output voltage range	• Transfer function: $V_{CSAOUT} = V_{CSAOUT\_OFF} + G * (V_{CSAP} - V_{CSAN})$ • Within this range the CSA characteristic is linear • Within this range the CSA errors are inside the specified limits
Output voltage offset range	• Defines V_{CSAOUT} under the condition $V_{CSAP} = V_{CSAN}$ • Determines the symmetry of input voltage range
Differential gain factor	• Nominal gain factors are 10, 20, 40, 60
Linearity error	• Maximum deviation from best fit line • 15 mV/1LSB12
Input differential mode offset	• Maximum differential input offset ($V_{CSAP} - V_{CSAN} = V_{INOFF}$) which is allowed to be added in order to get V_{CSAOUT_OFF} at the CSA output
Input resistance	Differential resistance between CSAP and CSAN input
Common mode rejection ratio	CMRR = -20*log(differential mode gain/common mode gain)
Output settling time	Settling time upon a wide input range swing (into the saturation range)
Settling time after power on	Time the CSA needs to settle after power on

18.3.2 Transfer characteristic and error definition

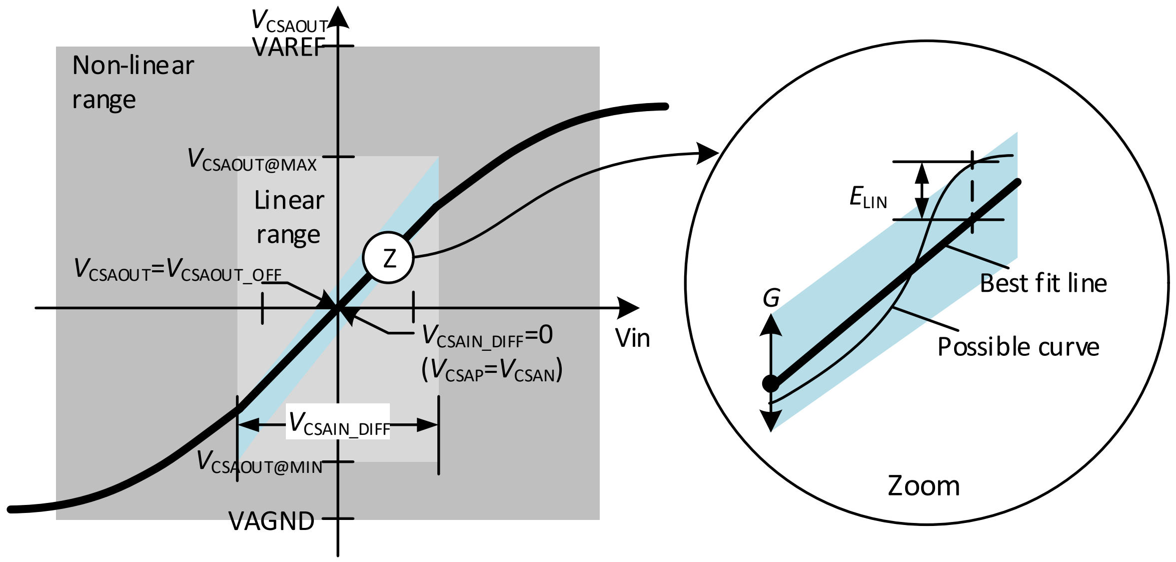


Figure 29 CSA transfer characteristic

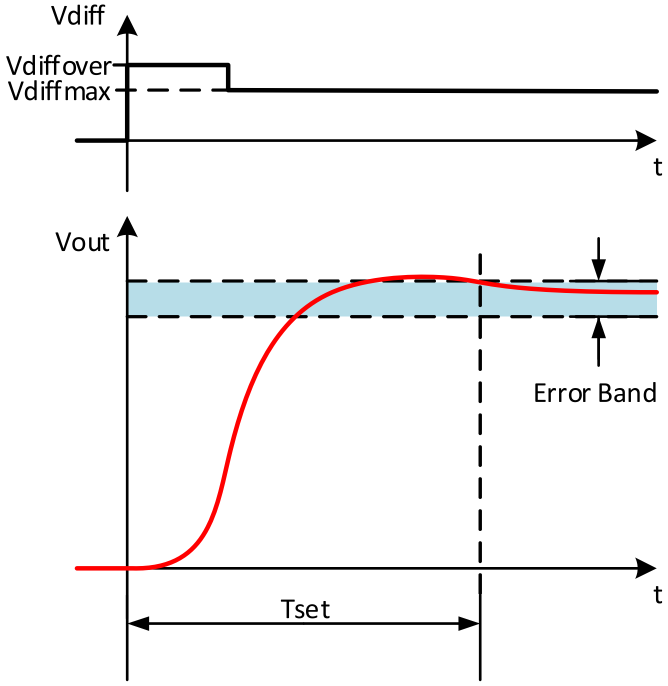


Figure 30 CSA settling time

18.3.3 CSA characteristics

Table 62 Electrical Characteristics Current Sense Amplifier

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Differential Linear Input Voltage Range	V_{CSAIN_DIFF}	0	-	3 / G	V	V_{CSAIN_DIFF}=V_{CSAP}-V_{CSAN}, minimum setting for V_{CSAOUT_OFF}	P_CSA_01_09
		-1.5 / G	-	1.5 / G	V	V_{CSAIN_DIFF}=V_{CSAP}-V_{CSAN}, maximum setting for V_{CSAOUT_OFF}	P_CSA_01_10
Common Mode Input Voltage Range	V_{CSAx_CM}	-2.0	-	2.0	V		P_CSA_01_11
Single-Ended Linear Output Voltage Range	V_{CSAOUT}	0.39	-	3.5	V		P_CSA_01_12
Output Voltage Offset	V_{CSAOUT_OFF}	0.45	0.5	0.55	V	CTRL2.OFFS_SEL<1:0>=00b	P_CSA_01_13
		0.95	1	1.05	V	CTRL2.OFFS_SEL<1:0>=01b	P_CSA_01_27
		1.45	1.5	1.55	V	CTRL2.OFFS_SEL<1:0>=10b	P_CSA_01_28
		1.95	2	2.05	V	CTRL2.OFFS_SEL<1:0>=11b	P_CSA_01_29
Differential Gain	G	9.85	10	10.15		CTRL2.GAIN_SEL<1:0>=00_B	P_CSA_01_14
		19.7	20	20.3		CTRL2.GAIN_SEL<1:0>=01_B	P_CSA_01_15
		39.4	40	40.6		CTRL2.GAIN_SEL<1:0>=10_B	P_CSA_01_16
		59.1	60	60.9		CTRL2.GAIN_SEL<1:0>=11_B	P_CSA_01_17
Linearity error	E_{LIN}	-15	-	15	mV	maximum deviation from best fit line; G=40	P_CSA_01_18
Input Differential Mode Offset	V_{INOFF}	-1.3	-	1.3	mV	G=40 ; V_{CSAN}=0V; V_{CSAP}=0V; CTRL2.OFFS_SEL<1:0>=00_B	P_CSA_01_19
		-3	-	3	mV		P_CSA_01_31
Additional Input Offset	V_{CSAIN_OFF}	-15%	20	+15%	mV	CTRL2.ADD_INP_OFFS=1b	P_CSA_01_30

Table 62 Electrical Characteristics Current Sense Amplifier (cont'd)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input Bias Current	I_{CSAx}	-300	-	0	µA	V_{CSAN}=0V; V_{CSAP}=0V	P_CSA_01_20
Input Resistance	R_{IN}	1	1.3	1.6	kΩ	Differential resistance between CSAP and CSAN	P_CSA_01_22
Common Mode Rejection Ratio	$CMRR_{CSA}$	58	80	-	dB	V_{CSAP}-V_{CSAN}=0V; -2V≤V_{CSAx}≤2V; G=40	P_CSA_01_24
Output Settling Time	T_{SET}	-	800	1400	ns	Time until the CSA output voltage settles and stays within the error band under all input conditions	P_CSA_01_25

19 Current Sense Comparator (CSC)

19.1 Features overview

The Current Sense Comparator (CSC) is used for fast detection and reaction on overcurrent on the shunt measurement by the CSA.

The CSC provides following features:

- The CSC compares the CSA output voltage against a programmable threshold voltage to detect positive overcurrents through the shunt
- The CSC threshold voltage is derived from the ADC1 reference voltage
- The CSC provides a programmable filter time
- The CSC event can trigger a CCU7.CTRAP event
- The CSC event can trigger an interrupt request
- The CSC event can switch off the bridge driver output safely (safe switch off in case of overcurrent)
- The CSC output status is indicated by a volatile level indication flag showing the actual status
- The CSC output status is indicated by a sticky status flag which must be cleared by software
- The CSC output status is indicated by an interrupt request flag

19.2 Block diagram

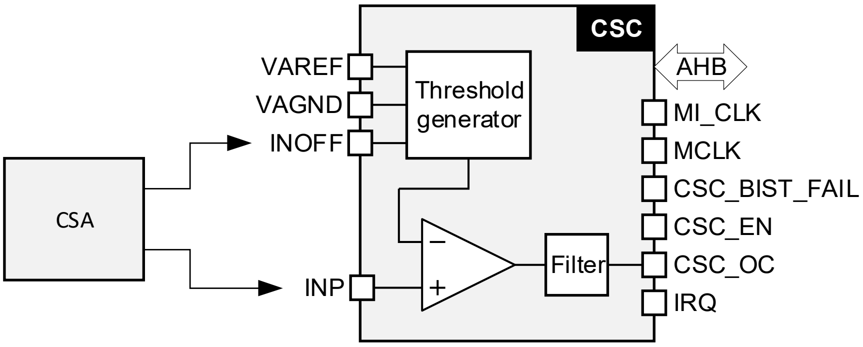


Figure 31 Block diagram CSC

19.3 Electrical characteristics CSC

19.3.1 CSC characteristics

Table 63 Electrical Characteristics Current Sense Comparator

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CSC overcurrent threshold	V_{CSC_THR}	V_{CSAOUT_OFF}	-	3.5	V	programmable by SFR	P_CSC_01_01
CSC filter time	t_{CSC_FILT}	1.7	2	2.3	µs	CTRL2.TFILT_SEL=00b	P_CSC_01_02
		3.6	4	4.4	µs	CTRL2.TFILT_SEL=01b	P_CSC_01_03
		5.5	6	6.5	µs	CTRL2.TFILT_SEL=10b	P_CSC_01_04
		7.5	8	8.5	µs	CTRL2.TFILT_SEL=11b	P_CSC_01_05
CSC reaction time	t_{CSC_REACT}	-	-	2	µs		P_CSC_01_10

20 Temperature Sensor Unit (TMPSNS)

20.1 Features overview

The SoC integrates multiple temperature sensors spread across the die. These monitors are located and associated with critical blocks such as:

- PMU module (VDDP and VDDEXT linear regulators)
- CAN transceiver module
- Gate driver module (2-stage charge pump), TEMP0
- SoC core logic, TEMP1

This chapter describes the behavior of the temperature sensors TEMP0 and TEMP1. The overtemperature protection mechanisms associated with the PMU and the CAN transceiver are described in the respective module chapters.

The TMPSNS provides following features:

- Two dedicated temperature sensors to measure the on-chip temperature at different locations:
  - TEMP0 measures the die temperature in the charge pump of gate driver module
  - TEMP1 measures the die temperature in the center of the chip (i.e. system temperature)
- Positive output slope of 2.5 mV/°C typ. over the full T_j = -40°C to +175°C temperature range
- Temperature sensors connect internally to the multiple inputs analog-to-digital converter (ADC2). The ADC2 post-processing and digital comparator features are used for background temperature monitoring
- ADC2 raises an overtemperature shutdown flag (CP_OT) when the die temperature in the charge pump (TEMP0) exceeds the threshold value (190°C typ.)
- ADC2 raises an overtemperature warning flag (SYS_OTWARN) when the system temperature (TEMP1) exceeds the threshold value (135°C typ.)
- ADC2 raises an overtemperature shutdown flag (SYS_OT) when the system temperature (TEMP1) exceeds the threshold value (190°C typ.). This event will automatically transition the SoC into Fail-sleep system power mode (refer to WAKE_FAIL_STS.SYS_OT bit description)

20.2 Block diagram

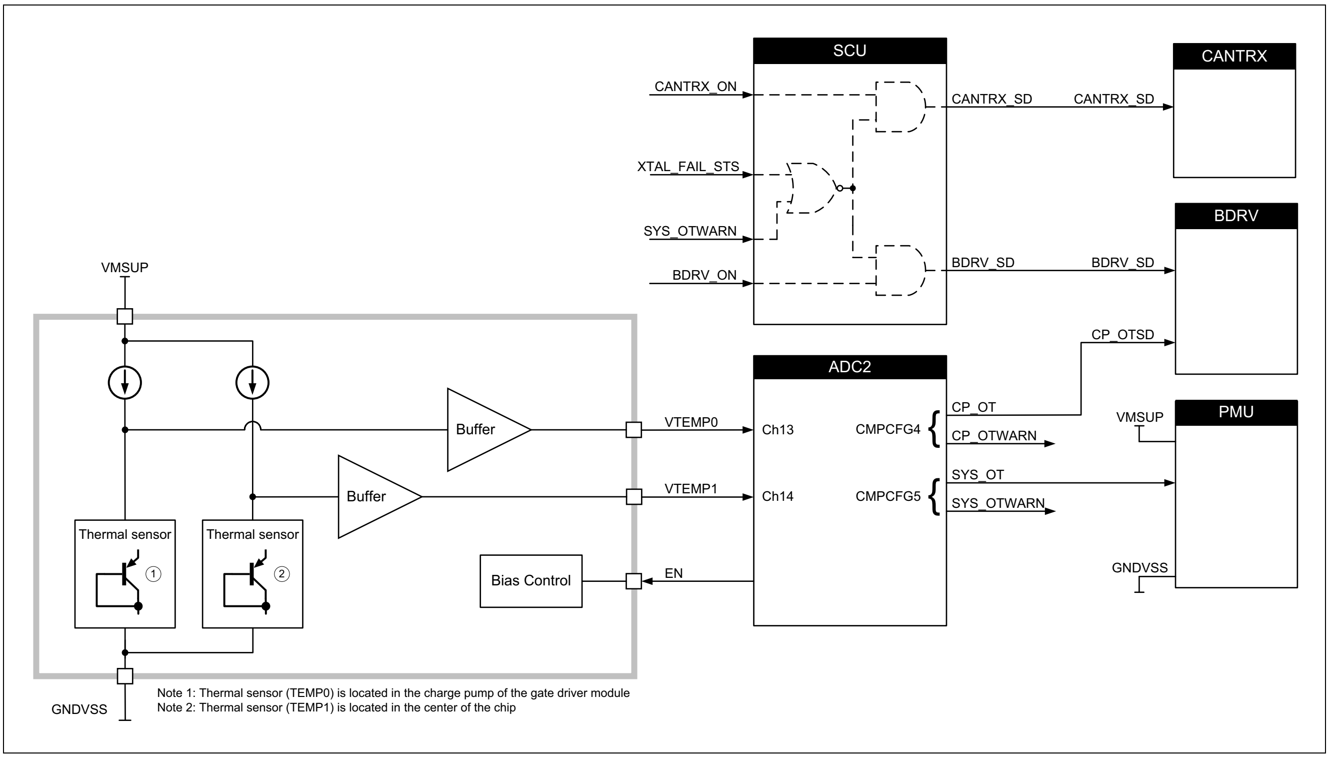


Figure 32 Block diagram TMPSNS

20.3 Electrical characteristics TMPSNS

20.3.1 TMPSNS characteristics

Table 64 Temperature Sensor Specifications

V_S = 3 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Accuracy 1	Acc_1	-10	-	10	K	-40°C<T_j<85°C	P_TEMP_02_04
Accuracy 2	Acc_2	-10	-	10	K	125°C<T_j<175°C	P_TEMP_02_05
Accuracy 3	Acc_3	-5	-	5	K	85°C≤T_j≤125°C	P_TEMP_02_06
Offset coefficient (a)	a	-	678	-	mV	1)	P_TEMP_02_07
Gain coefficient (b)	b	-	2.5	-	mV/°C	1)	P_TEMP_02_08

1) Not subject to production test, specified by design

Table 65 System Thermal Shutdown

V_S = 3 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
System Thermal Shutdown Threshold	$T_{j\_SYS\_TSD}$	180	190	200	°C		P_TEMP_03_01
Bridge Driver Thermal Shutdown Threshold	$T_{j\_BDRV\_TSD}$	180	190	200	°C		P_TEMP_03_02

21 BEMF Comparators (BEMFC)

21.1 Feature overview

For rotor position detection of a BLDC motor the BEMF (Back ElectroMotive Force) information can be used. This BEMF information is always sensed in the phase which is currently not active. Therefore, at each motor phase, a comparator compares the BEMF voltage against a virtual star point built by the other two motor phases and provides post-processing features to generate valid zero-crossing events.

The BEMFC provides following features:

- The BEMF comparator module consists of 3 BEMF comparators, one for each SHx pin
- The BEMF comparators compare the voltage at the corresponding SHx pin to a “virtual star point” voltage which is the average of the voltages at the remaining two SHy and SHz pins (see V_{BEMFC_TH})
- The BEMF comparators provide low settling time t_{BEMFC_D}
- The BEMF comparators can be switched off if not needed to avoid additional power consumption and undesired input currents in power down modes
- The BEMF comparator output signals are spike filtered with a programmable filter time
- The BEMF comparators have each a blanking filter which can be enabled to mask oscillations during a programmable time after switching the corresponding motor phases
- The BEMF comparators have each a demagnetisation filter which can be enabled to automatically remove demagnetisation pulses from the BEMF comparator output signal to get only valid zero-crossing events
- Interrupts can be triggered on BEMF comparator status changes at rising and/or falling edge

21.2 Block diagram

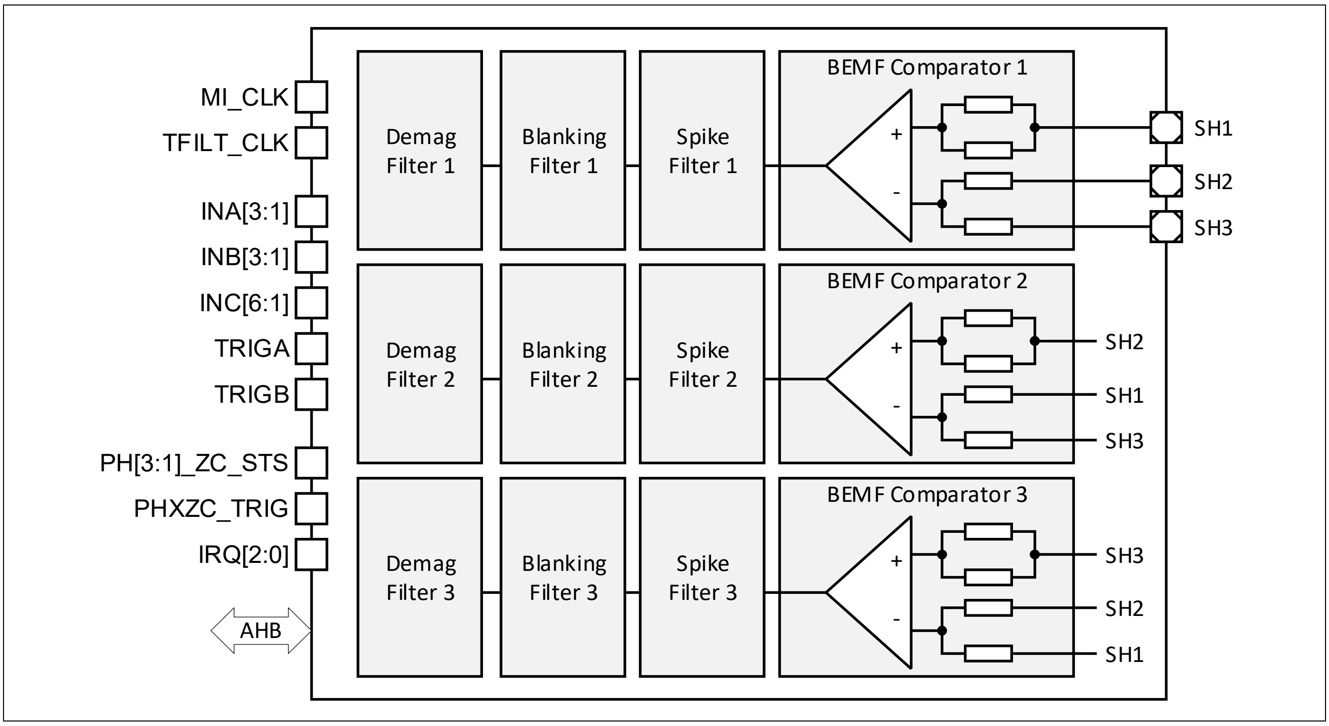


Figure 33 **Block diagram BEMFC**

21.3 Electrical characteristics BEMFC

21.3.1 Threshold and hysteresis

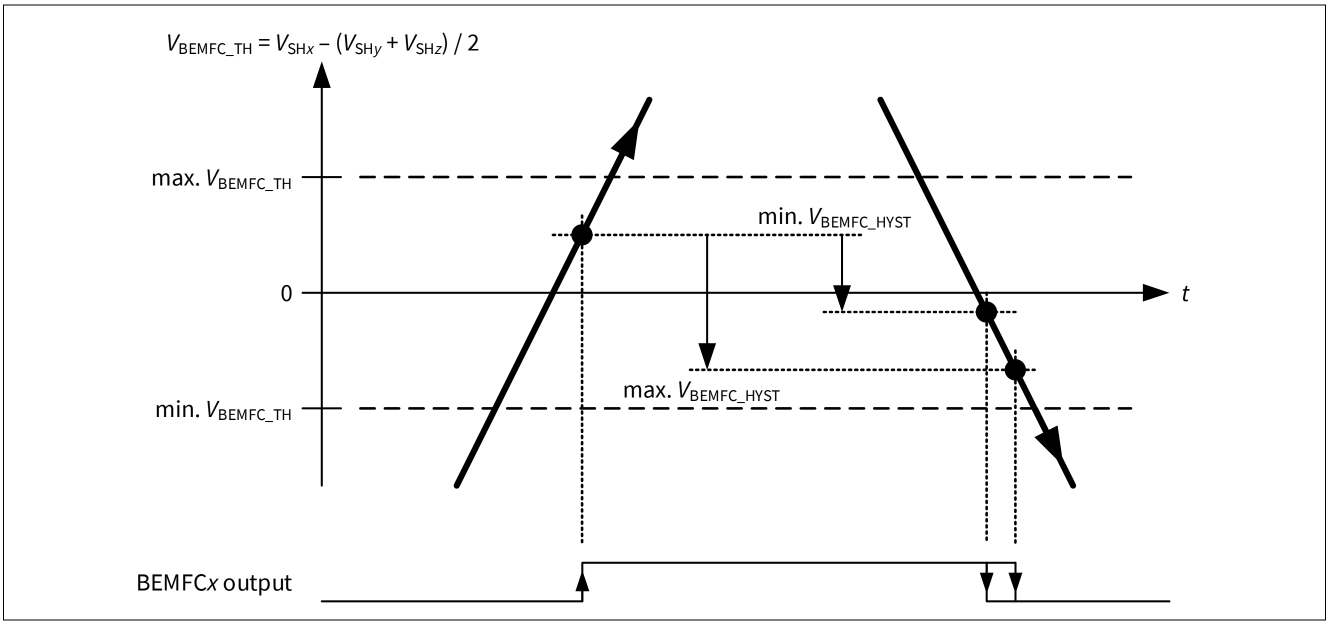


Figure 34 BEMFC threshold and hysteresis definition

21.3.2 BEMFC characteristics

Table 66 Electrical Characteristics

V_S = 4.4 V to 28 V, V_{SD} = 5.4 V to 29 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Detection threshold	V_{BEMFC_TH}	-50	-	50	mV	[1] [2]	P_BEMFC_01_01
Comparator hysteresis	V_{BEMFC_HYST}	5	-	40	mV		P_BEMFC_01_02
Comparator delay	t_{BEMFC_D}	-	-	1	µs	Voltage step on V_{SHx} from 0 V to V_{SD} + 500 mV; V_{SHy}=0V; V_{SHz}=V_{SD}	P_BEMFC_01_03

1) Comparison against "virtual star point": $V_{BEMFC\_TH} = V_{SHx} - (V_{SHy} + V_{SHz}) / 2$

2) Not subject to production test, specified by design

22 Sigma Delta ADC (SDADC)

22.1 Features overview

There is one Sigma Delta ADC (SDADC) module with two independent channels with input stage, 2nd order modulator, 3rd order CIC filter, result handling and synchronization feature. The SDADC is optimized for the usage of external AMR/GMR/TMR type sensors. The application configuration is shown in **Figure 35**, the block diagram in **Figure 36**.

The SDADC has following features:

- Performance
  - Sampling frequency up to 20 MHz (typ.), *MCLK*, f_S
  - Input frequency of up to 1 kHz (typ.), f_{IN}
  - Linear input range of ±3.75 V (typ.), V_{DIFF_lin}
  - RMS noise of less than 1 mV (typ.), V_{rms}
  - SNDR of 72 dB (typ.), *SNDR*
- Input stages
  - Configurable for differential or single ended input types
  - Two possible inputs selectable for usage of two sensors in time multiplex
  - Offset compensation feature
- Modulator (2nd order type)
  - Normal mode (use modulator and demodulator together)
  - External demodulator mode (modulator’s output as alternate function, demodulator external)
  - External modulator mode (modulator bypassed, demodulator inputs via GPIOs)
  - Dither unit for dead zone cancellation and idle tone reduction
- Demodulator (3rd order CIC filter type)
  - Linear programmable decimation factor (DECF) from 16 to 512 with automatic result scaling
  - 16-bit signed filter result (s16 format, internally s29)
  - Two filter modes: continues or triggered (synchronization feature to PWM)
  - Timestamping upon external trigger to capture the age of a result (synchronization feature to PWM)
  - Programmable digital comparator thresholds three modes (range, over-, undervoltage)
- Interrupts, DMA and events
  - SDADC events can be mapped to 2 interrupt node pointers (with 2 IRQ lines)
  - Result events can be mapped to 2 DMA requests
  - Compare events are connected to GPIOs, CCU7 and GPT12

22.2 Block diagram

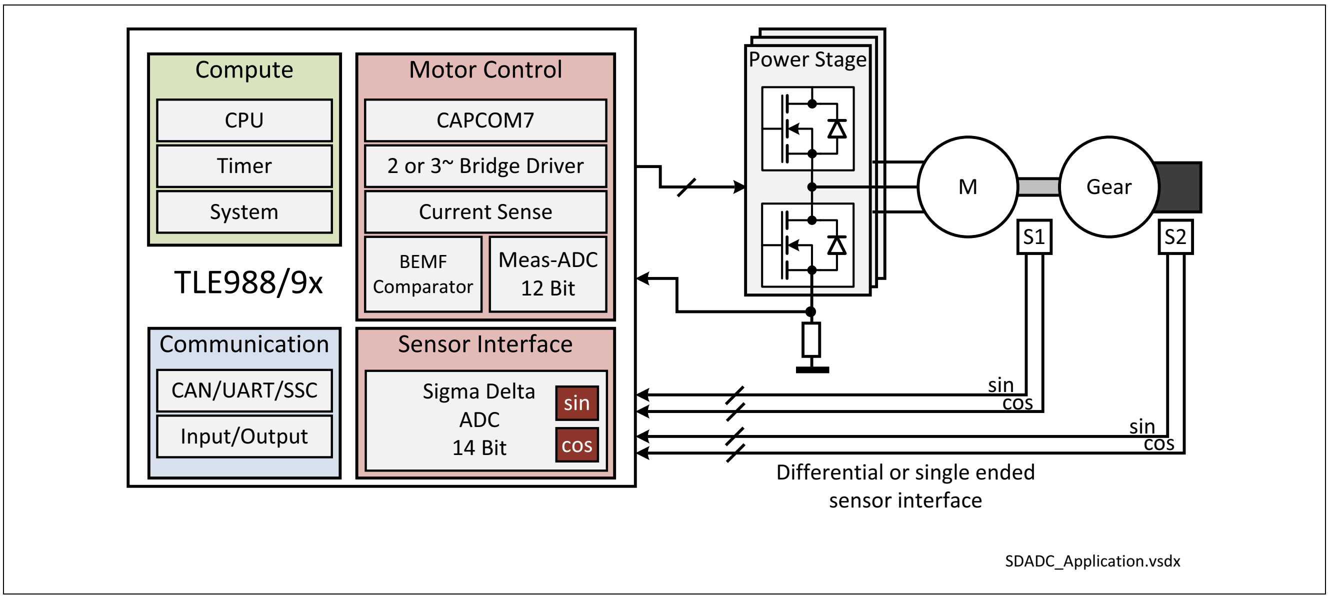


Figure 35 Application diagram SDADC

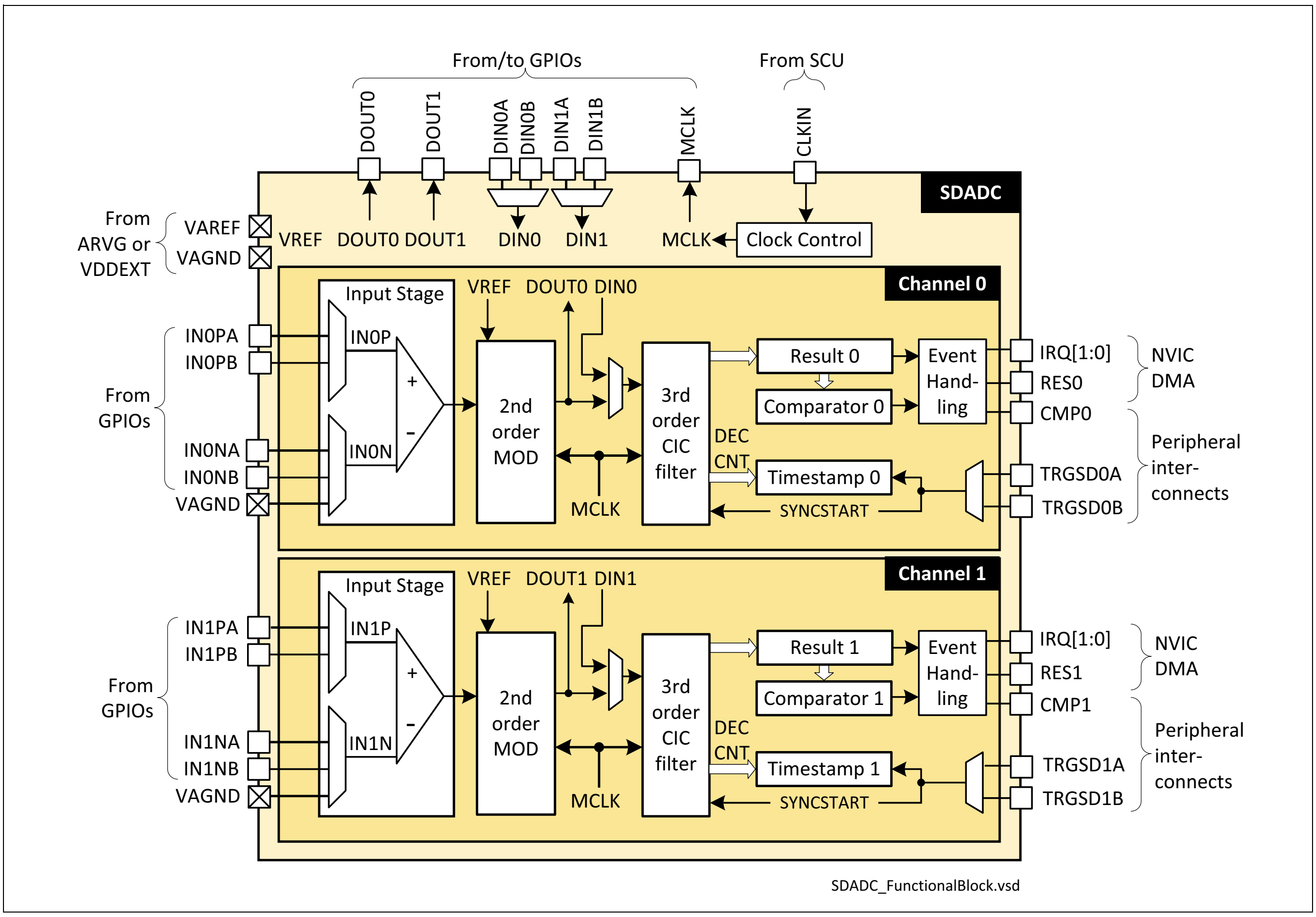


Figure 36 Block diagram SDADC

22.3 Electrical characteristics SDADC

22.3.1 SDADC characteristics

Table 67 SDADC characteristics

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Sampling frequency	f_S	5	-	20	MHz	f_S is identical to MCLK	P_SDADC_01_02
Decimation factor	*DECF*	16	-	512			P_SDADC_01_03
Input voltage	V_{IN}	0	-	*VAREF*	V	Input voltage on SDADC.INxP or SDADC.INxN x={0,1}	P_SDADC_01_04
Differential linear input voltage	V_{DIFF_lin}	-3.75	-	3.75	V	$V_{DIFF} = V_{INxP} - V_{INxN}$; V_{INxP}, V_{INxN} within V_{IN} range; x={0,1}	P_SDADC_01_06
Differential non-linear input voltage	V_{DIFF_nonlin}	-4	-	4	V	$V_{DIFF} = V_{INxP} - V_{INxN}$; V_{INxP}, V_{INxN} within V_{IN} range; x={0,1}	P_SDADC_01_07
Single ended linear input voltage	V_{SNGL_lin}	0	-	3.75	V	$V_{SNGL} = V_{INxP}$; $V_{INxN} = 0$ V; x={0,1}	P_SDADC_01_08
Single ended non-linear input voltage	V_{SNGL_nonlin}	0	-	4	V	$V_{SNGL} = V_{INxP}$; $V_{INxN} = 0$ V; x={0,1}	P_SDADC_01_09
Full scale voltage	V_{FS}	3.75	-	-	V	At $V_{DIFF} = \pm V_{FS}$; $RESULT_{max}$ resp. $RESULT_{min}$ is reached (defined as linear voltage range)	P_SDADC_01_10
Input frequency	f_{IN}	0	-	1	kHz		P_SDADC_01_11
RMS noise	V_{RMS}	-	0.69	2.4	mV	[1] Tested with DECF = 128 and VREF = VREF5V	P_SDADC_01_12
Effective resolution	*ERES*	10.61	12.4	-	Bits	[1] Calculated, ERES = $ld(V_{FS}/V_{RMS})$	P_SDADC_01_13
Effective number of bits	*ENOB*	-	11.7	-	Bits	[1] ENOB = (SNDR - 1.76dB) / 6.02dB	P_SDADC_01_14
SNDR with a fully differential sinus - 6dBFS	*SNDR*	-	72	-	dB	[1] Characterized, not tested in production	P_SDADC_01_15

Table 67 SDADC characteristics (cont'd)

V_S = 5.5 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Filter result linear range	$RESULT_{lin}$	-16384	-	16383	LSB	Linear range, represented in two's complement; RESULT= $(V_{DIFF} / V_{REF}) \times GAIN \times (2^{14} - 1)$	P_SDADC_01_16
Filter result non-linear range	$RESULT_{nonlin}$	-32768	-	32767	LSB	Linear range, represented in two's complement; RESULT= $(V_{DIFF} / V_{REF}) \times GAIN \times (2^{14} - 1)$	P_SDADC_01_17
Input gain	$GAIN$	-	4/3	-		[2]	P_SDADC_01_18
Gain ratio	G_R	0.99	-	1.01		$G_R = G_{CH0} / G_{CH1}$; channel mismatch due to gain mismatch	P_SDADC_01_19
Dynamic input impedance	Z_{IN}	0.1	0.25	1	MOhm	[1] $Z_{IN} = 1 / (2 \times f_S \times C_{IN})$	P_SDADC_01_21
Power up time	t_{up}	-	-	100	µs	Time after module RESET inactive to analog part in operating condition	P_SDADC_01_23
Coupling factor for negative overload current	$KOVAN$	-	-	0.0001		[3] [4] [1]	P_SDADC_01_24
Coupling factor for positive overload current	$KOVAP$	-	-	0.0001		[3] [1]	P_SDADC_01_25

1) Not subject to production test, specified by design

2) Defined by design

3) The overload coupling factor KOVAN/KOVAP (K) defines the worst case relation of an overload condition (Iov) at one pin to the resulting leakage current (Ileaktot) into an adjacent pin: Ileaktot = ±K × |Iov| + Ioz1. Thus the overload condition can cause an an additional error voltage at an adjacent analog input pin.

4) Overload current is allowed in following operation modes: unpowered, active and sleep mode.

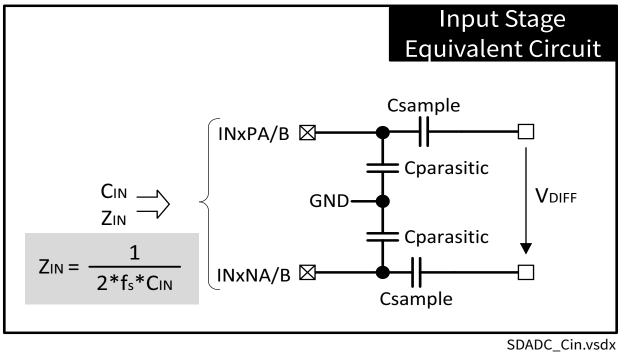


Figure 37 Input stage equivalent circuit

23 Timer20 (T20) and Timer21 (T21)

23.1 Features overview

Two functionally identical timers are implemented: Timer20 and Timer21. The description also use the name as Timer2.

The timer modules are general purpose 16-bit timers. Timer2 can function as a timer or counter in each of its modes. As a timer, it counts with an input clock of $f_{T2\_CLK}/12$ (if prescaler is disabled). As a counter, Timer2 counts 1-to-0 transitions on pin T2. In the counter mode, the maximum resolution for the count is $f_{T2\_CLK}/24$ (if prescaler is disabled).

The T20 and T21 provides following features:

- 16-bit auto-reload mode
  - selectable up or down counting
- One channel 16-bit capture mode
- T20 and T21 can be configured as trigger source for ADC1

23.1.1 Block diagram

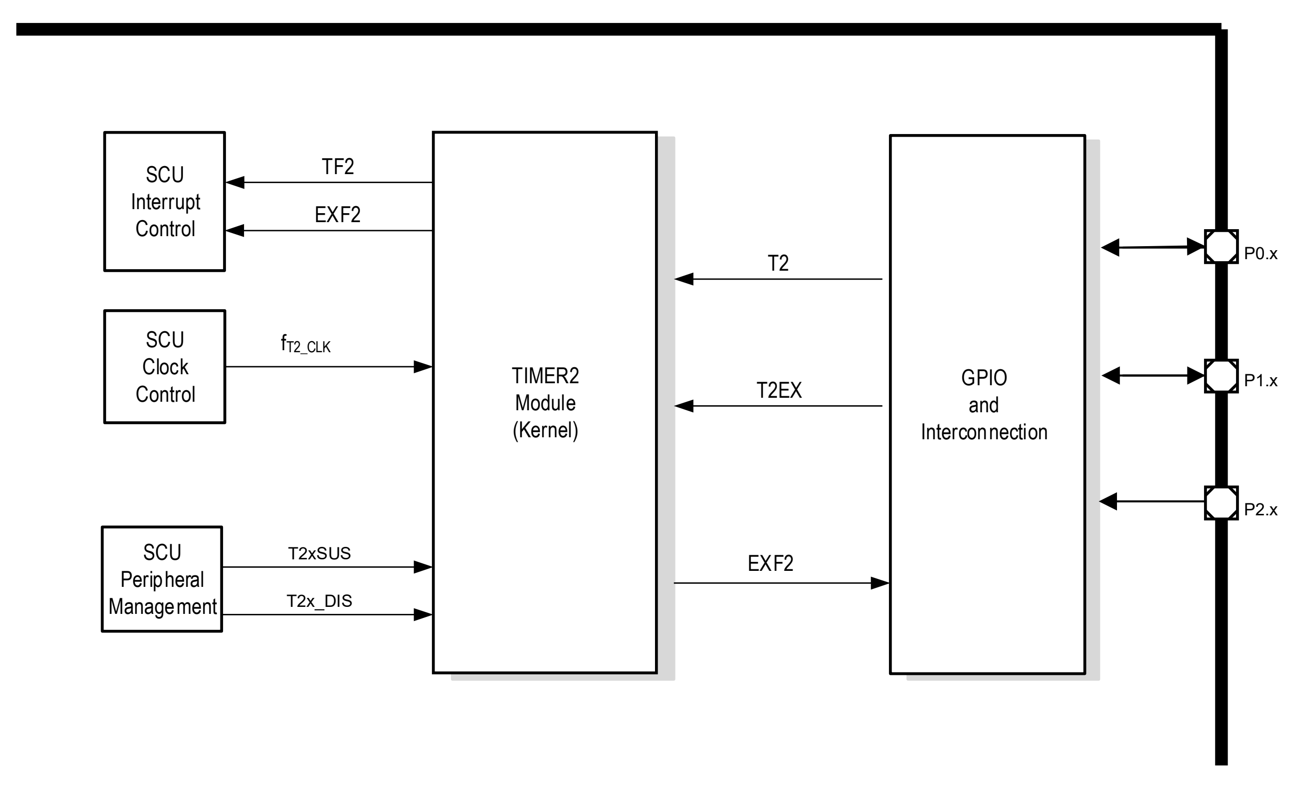


Figure 38 **Block diagram Timer2**

24 General Purpose Timer Units (GPT12)

24.1 Features overview

The General Purpose Timer Unit blocks GPT1 and GPT2 have very flexible multifunctional timer structures which may be used for timing, event counting, pulse width measurement, pulse generation, frequency multiplication, and other purposes.

They incorporate five 16-bit timers that are grouped into the two timer blocks GPT1 and GPT2. Each timer in each block may operate independently in a number of different modes such as Gated timer or Counter mode, or may be concatenated with another timer of the same block.

Each block has alternate input/output functions and specific interrupts associated with it. Input signals can be selected from several sources.

The GPT module is clocked with clock f_{GPT_CLK}.

The GPT12 provides following features:

- Features block GPT1:
  - $f_{GPT\_CLK}/4$ maximum resolution
  - 3 independent timers/counters
  - Timers/counters can be concatenated
  - 4 operating modes:
    - Timer mode
    - Gated Timer mode
    - Counter Mode
    - Incremental Interface mode
  - Reload and Capture functionality
- Features block GPT2:
  - $f_{GPT\_CLK}/2$ maximum resolution
  - 2 independent timers/counters
  - Timers/counters can be concatenated
  - 3 operating modes:
    - Timer mode
    - Gated Timer mode
    - Counter mode
  - Extended capture/reload functions

24.2 Block diagram

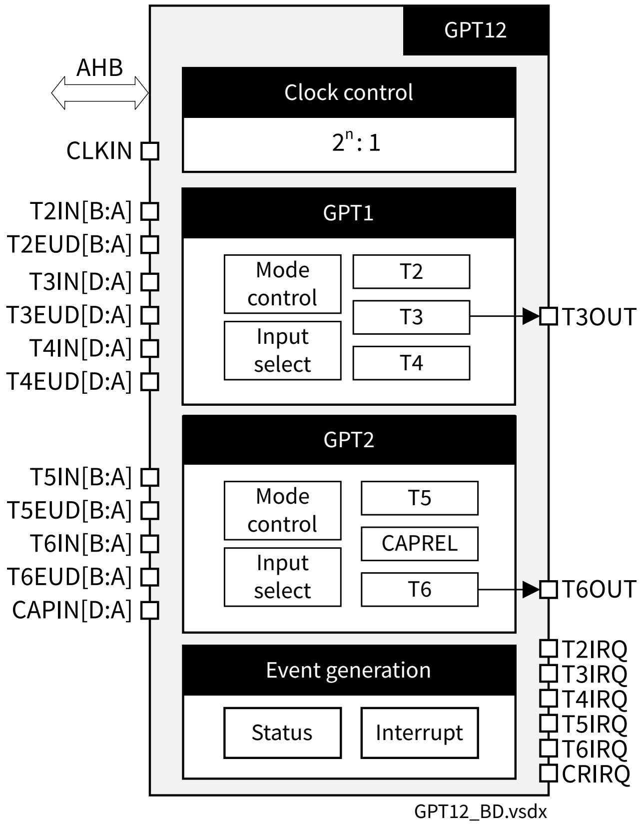


Figure 39 Block diagram GPT12

25 Capture/Compare Unit 7 (CCU7)

25.1 Features overview

The CCU7 is a high-resolution 16-bit capture and compare unit with application-specific modes, mainly for AC drive control. Special operating modes support the control of Brushless DC-motors using Hall sensors or Back-EMF detection. Furthermore, block commutation and control mechanisms for multi-phase machines are supported.

This chapter gives an overview over the different building blocks and their main features.

The CCU7 provides following features:

- Timer T12 block features:
  - Six compare channels
  - Supports generation of three-phase PWM (six outputs, individual signals for high-side and low-side switches)
  - 16-bit resolution, maximum count frequency (peripheral clock)
  - Dead-time control for each channel to avoid short-circuits in the power stage
  - Concurrent update of T12 registers
  - Center-aligned and edge-aligned PWM can be generated, as well as rising edge and duration PWM pulses
  - Single-shot mode supported
  - Start can be controlled by external events
  - Capability of counting external events
- Timer T13 block features:
  - One independent compare channel with one output
  - 16-bit resolution, maximum count frequency (peripheral clock)
  - Concurrent update of T13 registers
  - Can be synchronized to T12
  - Event generation at period-match and compare-match
  - Single-shot mode supported
  - Start can be controlled by external events
  - Capability of counting external events
- Timer T14, T15 and T16 block features:
  - Each with one independent compare channel with one output
  - 16-bit resolution, maximum count frequency (module clock)
  - Dead-time control for each channel to avoid short-circuits in the power stage
  - Concurrent update of T14, T15 and T16 registers
  - Can be synchronized to T12
  - Event generation at period-match and compare-match
  - Single-shot mode supported
  - Start can be controlled by external events
  - Capability of counting external events

- Additional specific functions:
  - Block commutation support for brushless DC-drives with programmable state pattern, event-triggered next state switching and background speed capture
  - Programmable Hall-sensor pattern detection with noise filter
  - Integrated error handling
  - Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
  - Control modes for multi-channel AC-drives
  - Output levels can be selected and adapted to the power stage

25.2 Block diagram

The CCU7 is comprised of a timer T12 block with six capture/compare channels, and a timer T13, T14, T15 and T16 block with one compare channel each. The T12 channels can independently generate PWM signals or accept capture triggers, or they can jointly generate control signal patterns to drive AC-motors or inverters.

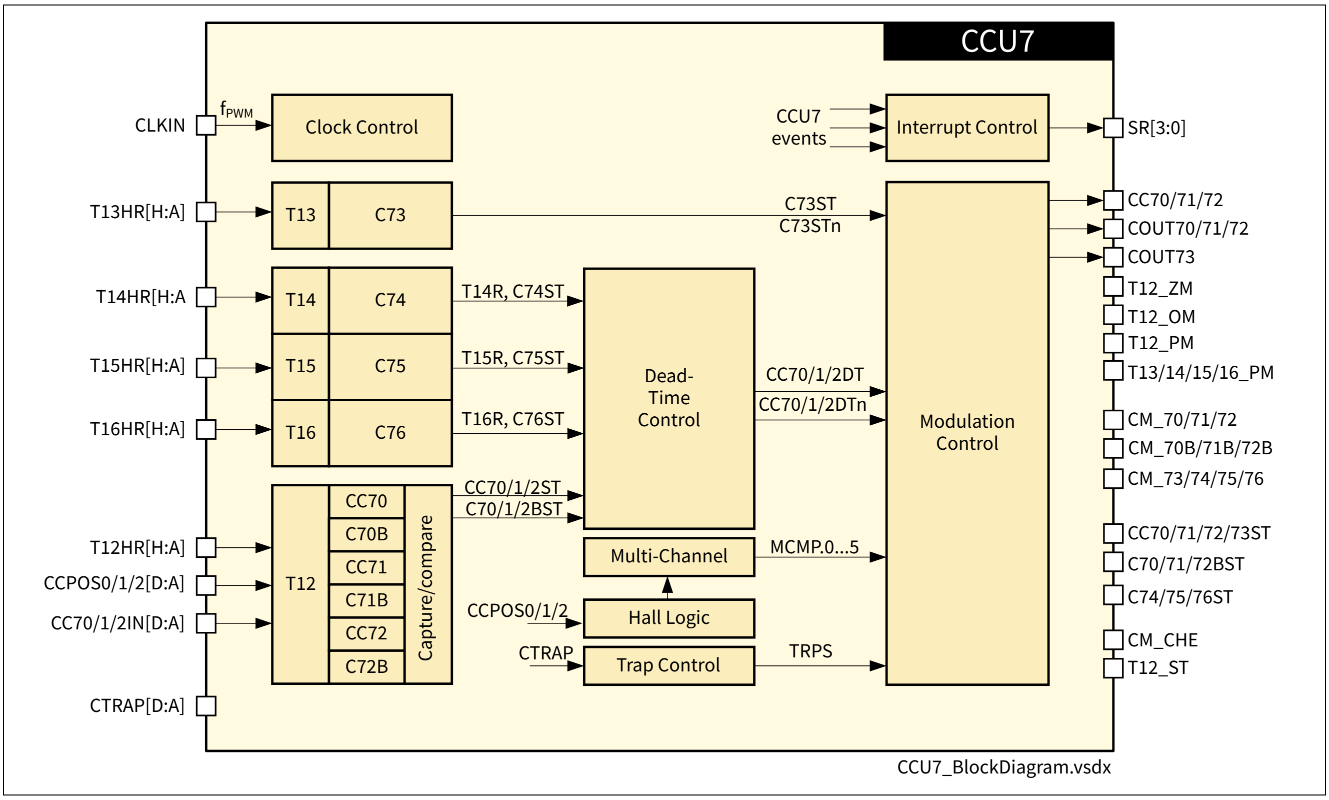


Figure 40 Block diagram CCU7

26 Bridge Driver (BDRV)

26.1 Features overview

The BDRV module consists of 6 gate drivers to control external normal-level n-channel MOSFETs arranged in 3 half bridges for 3-phase motor control applications.

The BDRV provides the following features:

- Flexible control by SFRs of Bridge Driver module, PWM output signals of CCU7 module, or alternate functions of GPIOs
- Current-driven output stages to control external n-channel MOSFET gates with flexibly programmable gate current profile
- Adjustable cross-conduction protection
- High-current discharge mode to reduce dead times and to keep external MOSFETs off during fast transients
- Safe switch-off path to switch off the Bridge Driver in a defined way in the case of errors
- Passive pull-down mode to keep external MOSFETs off if the Bridge Driver is disabled
- Active brake mode with reduced current consumption to statically switch on external MOSFETs
- Timing measurements of on/off delays and on/off slope durations
- Adaptive control mode with automatic adjustment of gate current values
- Integrated 2-stage charge pump for low-voltage operation and statical MOSFET gate control
- Adjustable voltage monitoring of Bridge Driver supply voltage (VSD) and charge pump output voltage (VCP)
- Adjustable short-circuit detection in on and off state
- Open-load detection in off state
- Overtemperature detection and shutdown

26.2 Block diagram

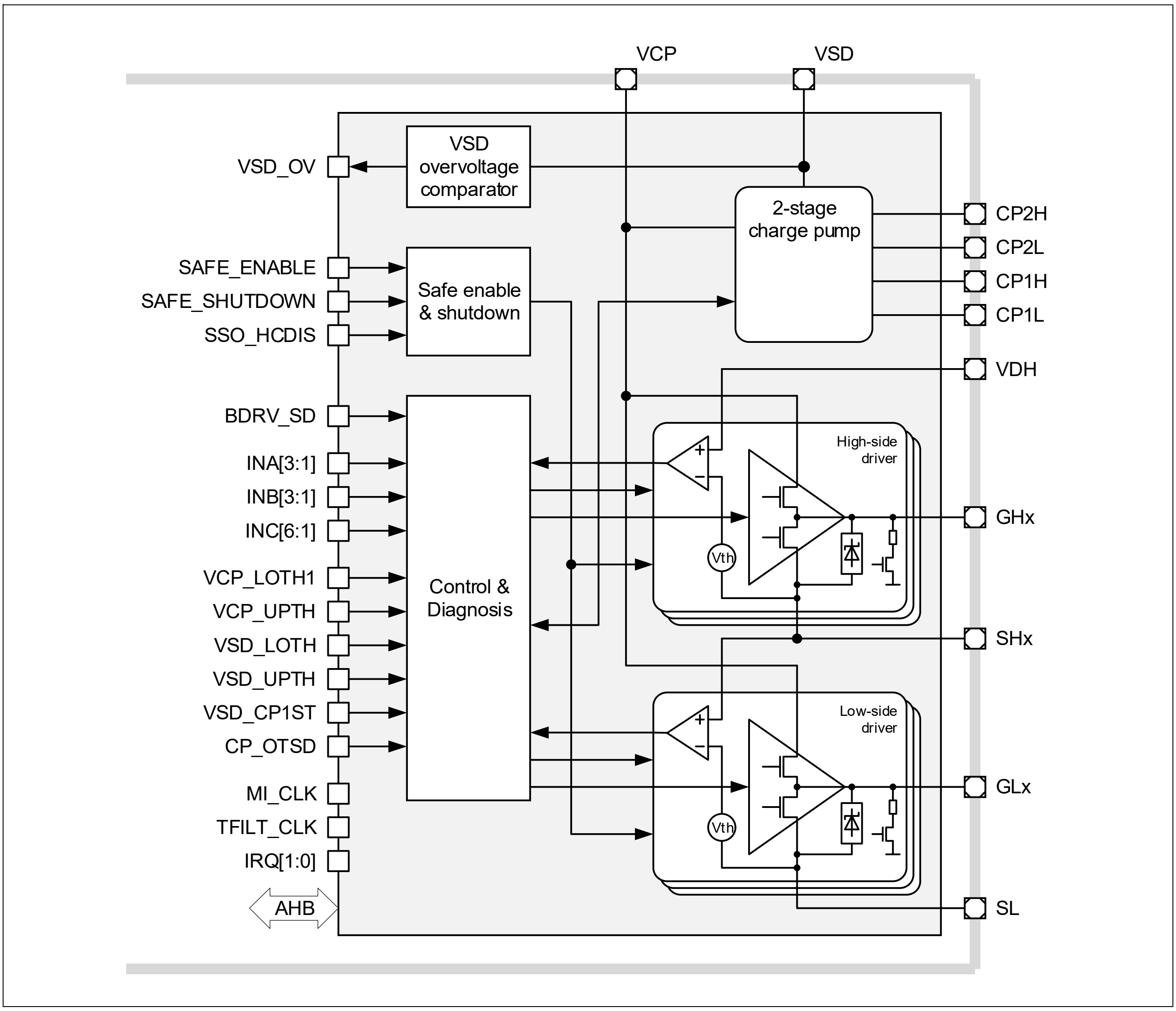


Figure 41 Block diagram BDRV

26.3 Electrical characteristics BDRV

26.3.1 Description of electrical parameters

26.3.1.1 Switch-on parameters

Figure 42 shows the detailed behavior of the gate driver output stage in the switch-on phase and the corresponding electrical characteristic parameters.

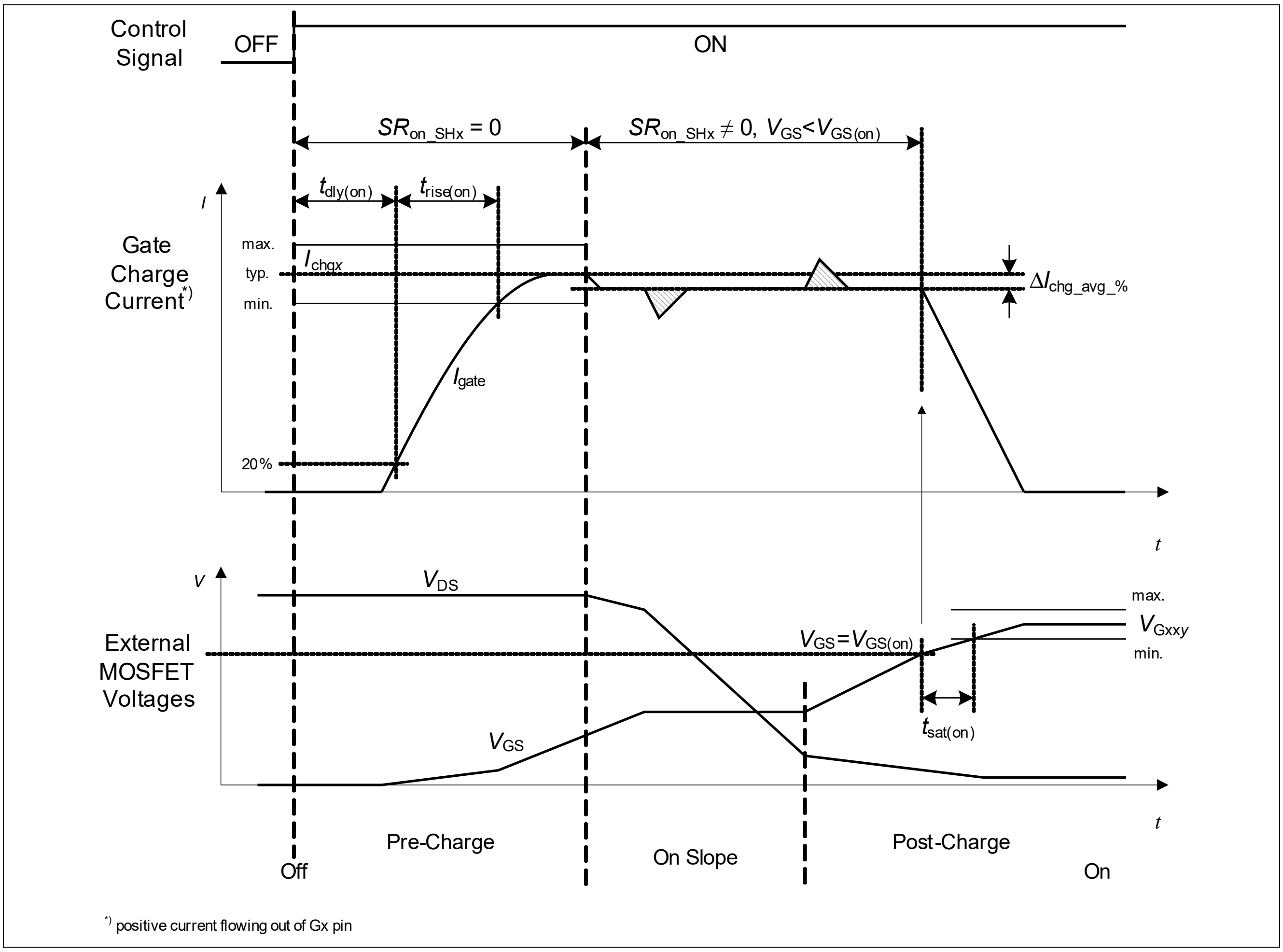


Figure 42 **Detailed behavior of the gate driver output stage in the switch-on phase**

After an initial turn-on delay time $t_{dly(on)}$ the gate charge current I_{gate} rises and after additional $t_{rise(on)}$ reaches its specified minimum limit $I_{chgx@MIN}$ and stays stable until the gate-to-source voltage of the external MOSFET reaches $V_{GS} = V_{GS(on)}$. During the slope at the corresponding SHx pin (i.e. the slew rate $SR_{on\_SHx} \neq 0$) the average gate current deviates less than $\Delta I_{chg\_avg\_\%}$ from the programmed nominal current I_{chgx}. The gate of the external MOSFET is further charged to the high-level output voltage of the gate driver V_{Gxxy}. The time from exceeding $V_{GS} = V_{GS(on)}$ and reaching $V_{Gxxy@MIN}$ is defined by $t_{sat(on)}$.

26.3.1.2 Switch-off parameters

Figure 43 shows the detailed behavior of the gate driver output stage in the switch-off phase and the corresponding electrical characteristic parameters.

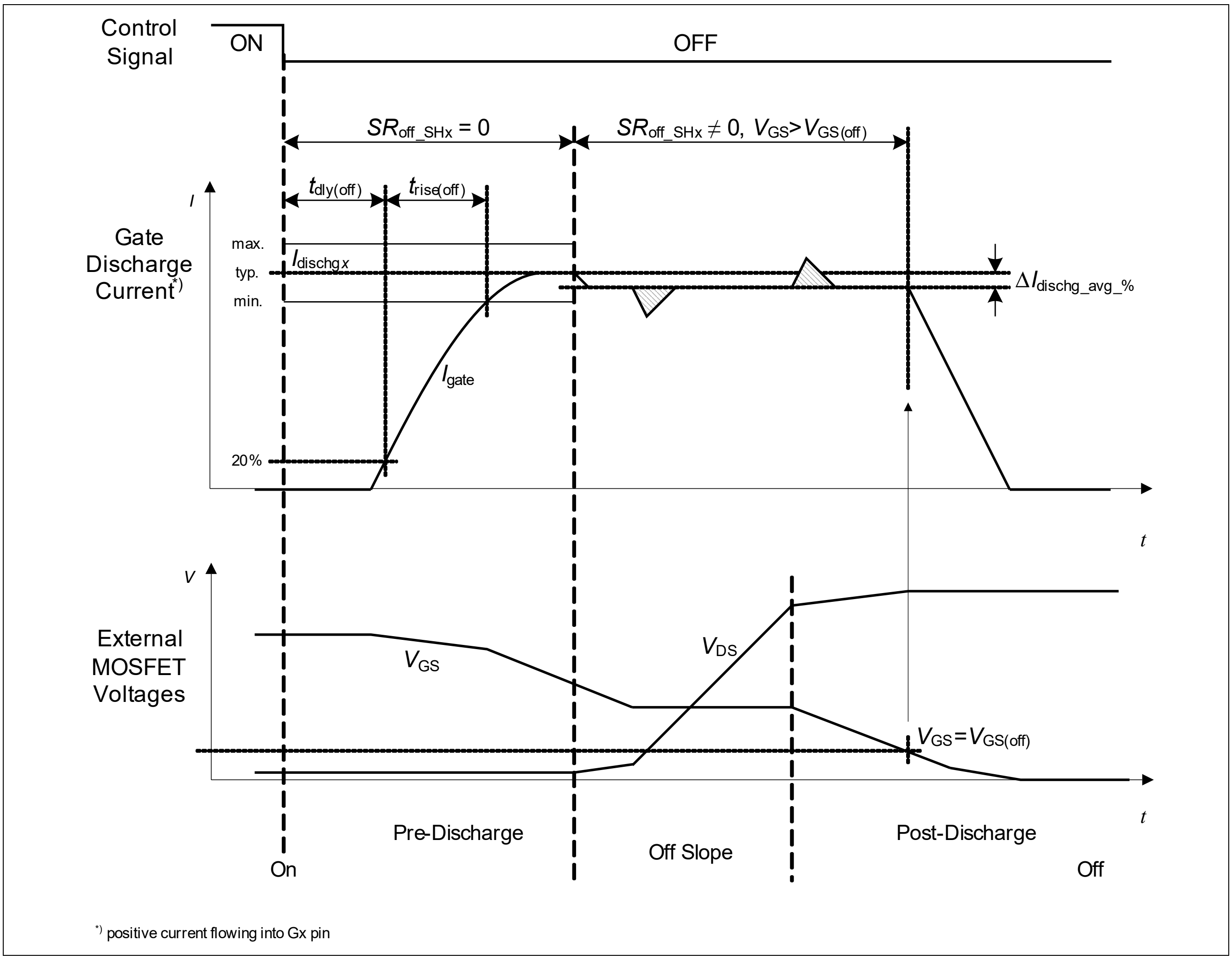


Figure 43 Detailed behavior of the gate driver output stage in the switch-off phase

After an initial turn-off delay time $t_{dly(off)}$ the gate discharge current I_{gate} rises and reaches its specified maximum limit $I_{dischg@MAX}$ after $t_{rise(off)}$ and stays stable until the gate-to-source voltage of the external MOSFET reaches $V_{GS} = V_{GS(off)}$. During the slope at the corresponding SHx pin (i.e. slew rate $SR_{off\_SHx} \neq 0$) the average gate discharge current deviates less than $\Delta I_{dischg\_avg\_\%}$ from the programmed nominal current $I_{dischgx}$.

26.3.1.3 Gate current settling behavior

At the transition between two different gate current value settings, the actual gate driver output current settles within $t_{set(seq)}$ to the new gate current value:

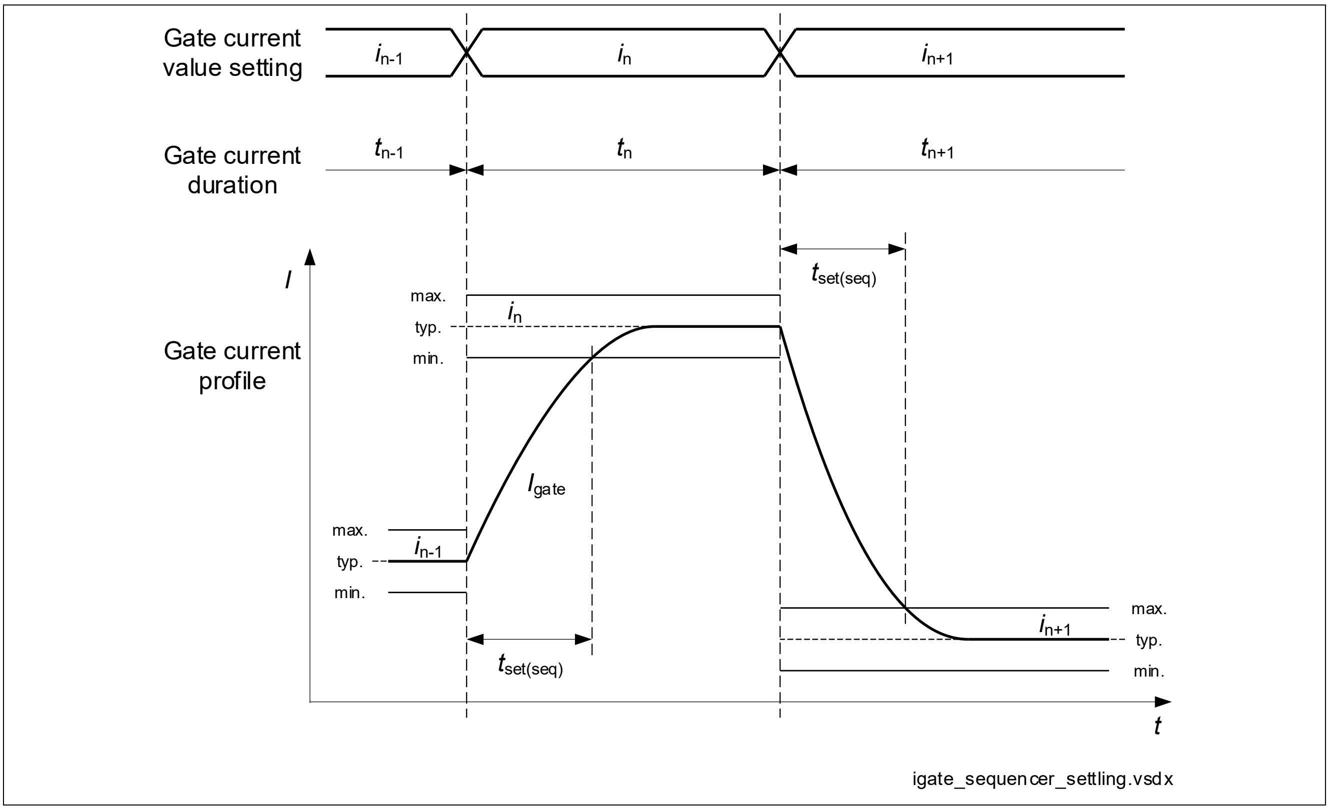


Figure 44 Gate current settling time

26.3.1.4 Timing measurement

Figure 45 shows the thresholds $V_{SH(high)}$ and $V_{SH(low)}$ and the propagation delays $t_{cdly(high)}$ and $t_{cdly(low)}$ of the high-speed voltage comparators during one PWM cycle of V_{SHx}:

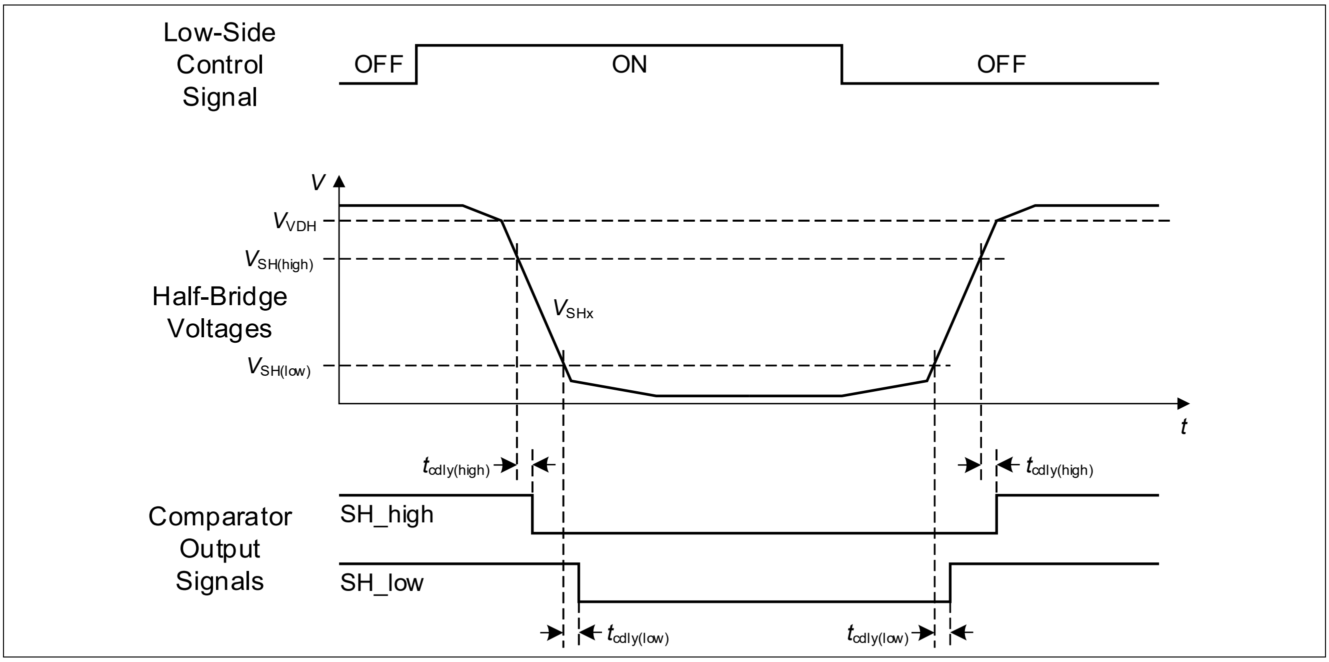


Figure 45 Timing measurement comparator thresholds and delays

26.3.2 MOSFET driver output characteristics

Table 68 MOSFET Driver Output

V_S = 4.4 V to 28 V, V_{SD} = 5.4 V to 29 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Gate charge current	I_{chg0}	1.5	4	8	mA	[1] $I_{CHARGE}=0_D$; $V_{GSx}≤V_{GS(on)}$; $V_{SD}≥8V$	P_BDRV_02_01
Gate charge current	I_{chg3}	5	10	15	mA	[1] $I_{CHARGE}=3_D$; $V_{GSx}≤V_{GS(on)}$; $V_{SD}≥8V$	P_BDRV_02_02
Gate charge current	I_{chg7}	12	18	24	mA	[1] $I_{CHARGE}=7_D$; $V_{GSx}≤V_{GS(on)}$; $V_{SD}≥8V$	P_BDRV_02_03
Gate charge current	I_{chg15}	33	45	57	mA	[1] $I_{CHARGE}=15_D$; $V_{GSx}≤V_{GS(on)}$; $V_{SD}≥8V$	P_BDRV_02_04
Gate charge current	I_{chg31}	100	125	150	mA	[1] $I_{CHARGE}=31_D$; $V_{GSx}≤V_{GS(on)}$; $V_{SD}≥8V$	P_BDRV_02_05
Gate charge current	I_{chg63}	290	340	390	mA	$I_{CHARGE}=63_D$; $V_{GSx}≤V_{GS(on)}$; $V_{SD}≥8V$	P_BDRV_02_06
Gate charge current dynamic average deviation	$\Delta I_{chg\_avg\_\%}$	-25%	-	+25%		[1] Reference: typ. I_{chgx}; SR_{on_SHx}=165V/µs; $V_{GSx}≤V_{GS(on)}$	P_BDRV_02_07
Gate discharge current	$I_{dischg0}$	1.5	5	8	mA	[1] $I_{DISCHARGE}=0_D$; $V_{GSx}≥V_{GS(off)}$; $V_{SD}≥8V$	P_BDRV_02_08
Gate discharge current	$I_{dischg3}$	5	10	15	mA	[1] $I_{DISCHARGE}=3_D$; $V_{GSx}≥V_{GS(off)}$; $V_{SD}≥8V$	P_BDRV_02_09
Gate discharge current	$I_{dischg7}$	13	20	27	mA	[1] $I_{DISCHARGE}=7_D$; $V_{GSx}≥V_{GS(off)}$; $V_{SD}≥8V$	P_BDRV_02_10
Gate discharge current	$I_{dischg15}$	37	50	63	mA	[1] $I_{DISCHARGE}=15_D$; $V_{GSx}≥V_{GS(off)}$; $V_{SD}≥8V$	P_BDRV_02_11
Gate discharge current	$I_{dischg31}$	100	125	150	mA	[1] $I_{DISCHARGE}=31_D$; $V_{GSx}≥V_{GS(off)}$; $V_{SD}≥8V$	P_BDRV_02_12
Gate discharge current	$I_{dischg63}$	310	360	410	mA	$I_{DISCHARGE}=63_D$; $V_{GSx}≥V_{GS(off)}$; $V_{SD}≥8V$	P_BDRV_02_13
Gate discharge current dynamic average deviation	$\Delta I_{dischg\_avg\_\%}$	-28%	-	+28%		[1] Reference: typ. $I_{dischgx}$; SR_{off_SHx}=165V/µs; $V_{GSx}≥V_{GS(off)}$; $V_{SD}≥8V$	P_BDRV_02_14
High level output voltage Gxx vs. Sxx	V_{Gxx1}	10	11	12	V	[2] All other drivers enabled but not ON; C_L=15nF; I_{CP}=18.9mA; R_{GS}=100kΩ; $V_{SD}≥8V$	P_BDRV_02_17

Table 68 MOSFET Driver Output (cont'd)

V_S = 4.4 V to 28 V, V_{SD} = 5.4 V to 29 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
High level output voltage Gxx vs. Sxx	V_{Gxx2}	7	-	12	V	2) All other drivers enabled but not ON; C_L=15nF; I_{CP}=16.2mA; R_{GS}=100kΩ; V_{SD}=7V	P_BDRV_02_18
High level output voltage Gxx vs. Sxx	V_{Gxx3}	7	-	12	V	2) All other drivers enabled but not ON; C_L=7nF; $I_{CHARGE} \le 31_D$; I_{CP}=7.6mA; R_{GS}=100kΩ; $T_j \le 150$°C; V_{SD}=5.4V	P_BDRV_02_20
High level output voltage GLx vs. GND / GHx vs. SHx - Active Brake Mode	V_{Gxx_ABK}	7	-	12	V	all other Drivers enabled but not ON; C_L=15nF; R_{GS}=100kΩ; V_{SD}=5.4V	P_BDRV_02_22
External MOSFET gate-to-source voltage - MOSFET on	$V_{GS(on)}$	5	-	-	V	1) V_{SD}=5.4V	P_BDRV_02_25
		7	-	-	V	1) V_{SD}=8V	P_BDRV_02_26
External MOSFET gate-to-source voltage - MOSFET off	$V_{GS(off)}$	-	-	2	V	1) $I_{DISCHARGE} < 31_D$	P_BDRV_02_27
		-	-	3.5	V	1) $I_{DISCHARGE} \ge 31_D$	P_BDRV_02_28
Rise time	t_{rise3_3nf}	40	70	100	ns	1) 25-75% of V_{Gxx1}; C_L=3.3nF; I_{CHARGE}=max ; $I_{DISCHARGE}$=max ; $V_{SD} \ge 8$V	P_BDRV_02_29
Fall time	t_{fall3_3nf}	40	70	100	ns	1) 75-25% of V_{Gxx1}; C_L=3.3nF; I_{CHARGE}=max ; $I_{DISCHARGE}$=max ; $V_{SD} \ge 8$V	P_BDRV_02_30
Rise time	$t_{risemax}$	50	-	350	ns	25-75% of V_{Gxx1}; C_L=10nF; I_{CHARGE}=max ; $I_{DISCHARGE}$=max ; $V_{SD} \ge 8$V	P_BDRV_02_31
Fall time	$t_{fallmax}$	50	-	350	ns	75-25% of V_{Gxx1}; C_L=10nF; I_{CHARGE}=max ; $I_{DISCHARGE}$=max ; $V_{SD} \ge 8$V	P_BDRV_02_32
Rise time	$t_{risemin}$	5	-	25	µs	1) 25-75% of V_{Gxx1}; C_L=10nF; I_{CHARGE}=min ; $I_{DISCHARGE}$=min ; $V_{SD} \ge 8$V	P_BDRV_02_33

Table 68 MOSFET Driver Output (cont'd)

V_S = 4.4 V to 28 V, V_{SD} = 5.4 V to 29 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Fall time	t_{fallmin}	5	-	25	µs	1) 75-25% of V_{Gxx1}; C_{L}=10nF; I_{CHARGE}=min ; $I_{\mathrm{DISCHARGE}}$=min ; $V_{\mathrm{SD}}\geq$8V	P_BDRV_02_34
Absolute rise - fall time difference for all LSx	$t_{\mathrm{r\_f(diff)LSx}}$	-	-	100	ns	25-75% of V_{Gxx1}; C_{L}=10nF; I_{CHARGE}=max ; $I_{\mathrm{DISCHARGE}}$=max ; $V_{\mathrm{SD}}\geq$8V	P_BDRV_02_35
Absolute rise - fall time difference for all HSx	$t_{\mathrm{r\_f(diff)HSx}}$	-	-	100	ns	25-75% of V_{Gxx1}; C_{L}=10nF; I_{CHARGE}=max ; $I_{\mathrm{DISCHARGE}}$=max ; $V_{\mathrm{SD}}\geq$8V	P_BDRV_02_36
Resistor between GHx/GLx and GND	R_{GGND}	10	13.5	17	kOhm		P_BDRV_02_38
Resistor between SHx and GND	R_{SHGN}	15	20	27	kOhm	3) This resistance is the resistance between GHx and GND connected through a diode to SHx. As a consequence the voltage at SHx can rise up to 0,6V typ. before it gets discharged through the resistor.	P_BDRV_02_39
Effective dischargeRDSON	R_{ONCCP}	2.5	5	10	Ohm	50mA forced into Gx, Sx grounded; $I_{\mathrm{DISCHARGE}}=63_{\mathrm{D}}$; $V_{\mathrm{CP}}=V_{\mathrm{SD}}$ +14.0V; V_{SD}=13.5V	P_BDRV_02_40
Input propagation time (LS on)	$t_{\mathrm{P(ILN)min}}$	3	-	12	µs	1) "ON"=1 to 25% of V_{Gxx1}; C_{L}=10nF; I_{CHARGE}=min	P_BDRV_02_42
Input propagation time (LS off)	$t_{\mathrm{P(ILF)min}}$	3	-	12	µs	1) "ON"=0 to 75% of V_{Gxx1}; C_{L}=10nF; $I_{\mathrm{DISCHARGE}}$=min	P_BDRV_02_43
Input propagation time (HS on)	$t_{\mathrm{P(IHN)min}}$	3	-	12	µs	1) "ON"=1 to 25% of V_{Gxx1}; C_{L}=10nF; I_{CHARGE}=min	P_BDRV_02_44
Input propagation time (HS off)	$t_{\mathrm{P(IHF)min}}$	3	-	12	µs	1) "ON"=0 to 75% of V_{Gxx1}; C_{L}=10nF; $I_{\mathrm{DISCHARGE}}$=min	P_BDRV_02_45
Input propagation time (LS on)	$t_{\mathrm{P(ILN)max}}$	-	200	350	ns	"ON"=1 to 25% of V_{Gxx1}; C_{L}=10nF; I_{CHARGE}=max	P_BDRV_02_46

Table 68 MOSFET Driver Output (cont'd)

V_S = 4.4 V to 28 V, V_{SD} = 5.4 V to 29 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input propagation time (LS off)	$t_{P(ILF)max}$	-	200	300	ns	"ON"=0 to 75% of V_{Gxx1}; C_L=10nF; $I_{DISCHARGE}$=max	P_BDRV_02_47
Input propagation time (HS on)	$t_{P(IHN)max}$	-	200	350	ns	"ON"=1 to 25% of V_{Gxx1}; C_L=10nF; I_{CHARGE}=max	P_BDRV_02_48
Input propagation time (HS off)	$t_{P(IHF)max}$	-	200	300	ns	"ON"=0 to 75% of V_{Gxx1}; C_L=10nF; $I_{DISCHARGE}$=max	P_BDRV_02_49
Absolute input propagation time difference between propagation times for all LSx (LSx on)	$t_{Pon(diff)LSx}$	-	-	100	ns	"ON"=1 to 25% of V_{Gxx1}; C_L=10nF; I_{CHARGE}=max	P_BDRV_02_50
Absolute input propagation time difference between propagation times for all LSx (LSx off)	$t_{Poff(diff)LSx}$	-	-	100	ns	"ON"=0 to 75% of V_{Gxx1}; C_L=10nF; $I_{DISCHARGE}$=max	P_BDRV_02_51
Absolute input propagation time difference between propagation times for all HSx (HSx on)	$t_{Pon(diff)HSx}$	-	-	100	ns	"ON"=1 to 25% of V_{Gxx1}; C_L=10nF; I_{CHARGE}=max	P_BDRV_02_52
Absolute input propagation time difference between propagation times for all HSx (HSx off)	$t_{Poff(diff)HSx}$	-	-	100	ns	"ON"=0 to 75% of V_{Gxx1}; C_L=10nF; $I_{DISCHARGE}$=max	P_BDRV_02_53

1) Not subject to production test, specified by design

2) The value of I_{CP} replicates the average load on the charge pump coming from 20-kHz PWM operation of 6 MOSFETs, having each a max. gate capacitance of the specified C_L, under the assumption that the low-side gates are charged up to $V_{Gxx1@TYP}$ and the high-side gates are charged up to the respective $V_{Gxxy@MIN}$.

3) This resistance is connected through a diode between SHx and GHx to ground.

26.3.3 Charge-discharge current timing characteristics

Table 69 Charge-Discharge Current Timing Characteristics

V_S = 4.4 V to 28 V, V_{SD} = 5.4 V to 29 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Charge current delay time	$t_{dly(on)}$	-	35	90	ns	[1] from "ON"=1 to 20% of I_{chgx} (x=0...63); C_L=10nF	P_BDRV_03_01
Charge current rise time	$t_{rise(on)}$	-	35	70	ns	[1] from 20% of I_{chgx} to $I_{chgx@MIN}$ (x=0...63); C_L=10nF	P_BDRV_03_02
Gate Source Voltage Saturation Time	$t_{sat(on)}$	-	50	100	ns	[1] from V_{GS}=$V_{GS(on)}$ to 0.9*$V_{Gxxy@MIN}$; C_L=10nF; I_{CHARGE}=63 ; V_{SD}≥8V	P_BDRV_03_03
Charge current settling time - sequencer mode	$t_{set\_chg(seq)}$	-	-	150	ns	[2] [1] from any $I_{CHARGE(n)}$ to $I_{CHARGE(n+1)}$ = 0_D or 63_D; C_L=10nF	P_BDRV_03_04
Discharge current settling time - sequencer mode	$t_{set\_dischg(seq)}$	-	-	75	ns	[3] [1] from any $I_{DISCHARGE(n)}$ to $I_{DISCHARGE(n+1)}$ = 0_D or 63_D; C_L=10nF	P_BDRV_03_05
Discharge current delay time	$t_{dly(off)}$	-	25	80	ns	[1] from "ON"=0 to 20% of $I_{dischgx}$ (x=0...63); C_L=10nF	P_BDRV_03_06
Discharge current rise time	$t_{rise(off)}$	-	25	70	ns	[1] from 20% of $I_{dischgx}$ to $I_{dischgx@MIN}$ (x=0...63); C_L=10nF	P_BDRV_03_07

1) Not subject to production test, specified by design

2) $I_{CHARGE(n)}$ and $I_{CHARGE(n+1)}$ are consecutive gate charge current set points in sequencer mode.

3) $I_{DISCHARGE(n)}$ and $I_{DISCHARGE(n+1)}$ are consecutive gate discharge current set points in sequencer mode.

26.3.4 Timing measurement comparators characteristics

Table 70 Timing Measurement Comparators

V_S = 4.4 V to 28 V, V_{SD} = 5.4 V to 29 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Low-side timing measurement comparator threshold voltage	$V_{SH(low)}$	2	-	2.5	V		P_BDRV_04_01
High-side timing measurement comparator threshold voltage	$V_{SH(high)}$	V_{SD}-2.5V	-	V_{SD}-2V	V		P_BDRV_04_02
Delay of low-side timing measurement comparator	$t_{cdly(low)}$	5	-	20	ns	[1]	P_BDRV_04_03
Delay of high-side timing measurement comparator	$t_{cdly(high)}$	5	-	25	ns	[1]	P_BDRV_04_04

1) Not subject to production test, specified by design

26.3.5 Drain source monitoring characteristics

Table 71 Drain source monitoring

V_S = 4.4 V to 28 V, V_{SD} = 5.4 V to 29 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Drain source monitoring threshold	$V_{DSMONVTH}$	-25%	0.125	+25%	V	BDRV_CTRL3.DSMONVTH<2:0>=000_B	P_BDRV_05_01
		-20%	0.25	+20%	V	[1] BDRV_CTRL3.DSMONVTH<2:0>=001_B	P_BDRV_05_02
		-15%	0.5	+15%	V	[1] BDRV_CTRL3.DSMONVTH<2:0>=010_B	P_BDRV_05_03
		-15%	0.75	+15%	V	[1] BDRV_CTRL3.DSMONVTH<2:0>=011_B	P_BDRV_05_04
		-15%	1.00	+15%	V	[1] BDRV_CTRL3.DSMONVTH<2:0>=100_B	P_BDRV_05_05
		-15%	1.25	+15%	V	[1] BDRV_CTRL3.DSMONVTH<2:0>=101_B	P_BDRV_05_06
		-15%	1.5	+15%	V	[1] BDRV_CTRL3.DSMONVTH<2:0>=110_B	P_BDRV_05_07
		-15%	1.75	+15%	V	[1] BDRV_CTRL3.DSMONVTH<2:0>=111_B	P_BDRV_05_08
Drain source monitoring filter time	t_{DS_FILT}	0.7	1	1.3	µs	[1] SFR setting 0	P_BDRV_05_09
		1.7	2	2.3	µs	[1] SFR setting 1	P_BDRV_05_10
		3.6	4	4.4	µs	[1] SFR setting 2	P_BDRV_05_11
		7.5	8	8.5	µs	[1] SFR setting 3	P_BDRV_05_12
Drain source monitoring blanking time	t_{DS_BLANK}	0.7	1	1.3	µs	[1] SFR setting 0	P_BDRV_05_13
		1.7	2	2.3	µs	[1] SFR setting 1	P_BDRV_05_14
		3.6	4	4.4	µs	[1] SFR setting 2	P_BDRV_05_15
		7.5	8	8.5	µs	[1] SFR setting 3	P_BDRV_05_16

1) Not subject to production test, specified by design

26.3.6 Open load diagnosis currents characteristics

Table 72 Open load diagnosis currents

V_S = 4.4 V to 28 V, V_{SD} = 5.4 V to 29 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Pull-Up diagnosis current	I_{PUDiag}	-750	-	-350	µA	$I_{DISCHARGE}$=0 ; V_{SD}≥6.4V; V_{SHx}=5V; V_s≥5.4V	P_BDRV_06_01
Pull-Down diagnosis current	I_{PDDiag}	900	-	1600	µA	$I_{DISCHARGE}$=0 ; V_{SD}≥6.4V; V_{SHx}=5V; V_s≥5.4V	P_BDRV_06_02
Effective Pull-Down diagnosis current overdrive	I_{PDDiag_OD}	200	-	-	µA	$I_{DISCHARGE}$=0 ; V_{SD}≥6.4V; V_{SHx}=5V; V_s≥5.4V	P_BDRV_06_03

26.3.7 Charge pump characteristics

Table 73 Charge pump

V_S = 4.4 V to 28 V, V_{SD} = 5.4 V to 29 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage VCP vs. VSD	V_{CPmin1}	8	-	11	V	[1] Bridge Driver enabled but not ON; C_{CP1}=220nF; C_{CP2}=220nF; I_{CP}=7.6mA; V_{SD}=5.4V; f_{CP}=250kHz	P_BDRV_07_01
Single-Stage Mode Output voltage VCP vs. VSD	$V_{CPsingle}$	11.7	-	16	V	[1] Bridge Driver enabled but not ON, Charge Pump in single-stage mode; C_{CP1}=220nF; C_{CP2}=220nF; I_{CP}=18.9mA; V_{SD}=18V; f_{CP}=250kHz	P_BDRV_07_02
Regulated output voltage VCP vs. VSD	V_{CP}	11.7	-	16	V	[1] Bridge Driver enabled but not ON; C_{CP1}=220nF; C_{CP2}=220nF; I_{CP}=18.9mA; V_{SD}≥8V; f_{CP}=250kHz	P_BDRV_07_03

Table 73 Charge pump (cont'd)

V_S = 4.4 V to 28 V, V_{SD} = 5.4 V to 29 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Turn ON Time	t_{ON_VCP}	10	-	70	µs	[2] [1] from CPCLK_EN='1' to 25% of V_{CP}; C_{CP1}=220nF; C_{CP2}=220nF; C_{VCP}=470nF; V_{SD}≥8V; f_{CP}=250kHz	P_BDRV_07_04
Rise time	t_{rise_VCP}	20	-	96	µs	[2] [1] from 25% to 75% of V_{CP}; C_{CP1}=220nF; C_{CP2}=220nF; C_{VCP}=470nF; V_{SD}≥8V; f_{CP}=250kHz	P_BDRV_07_05

1) Not subject to production test, specified by design

2) This time applies when bit DRV_CP_CLK_CTRL.CPCLK_EN is set

26.3.8 VSD overvoltage characteristics

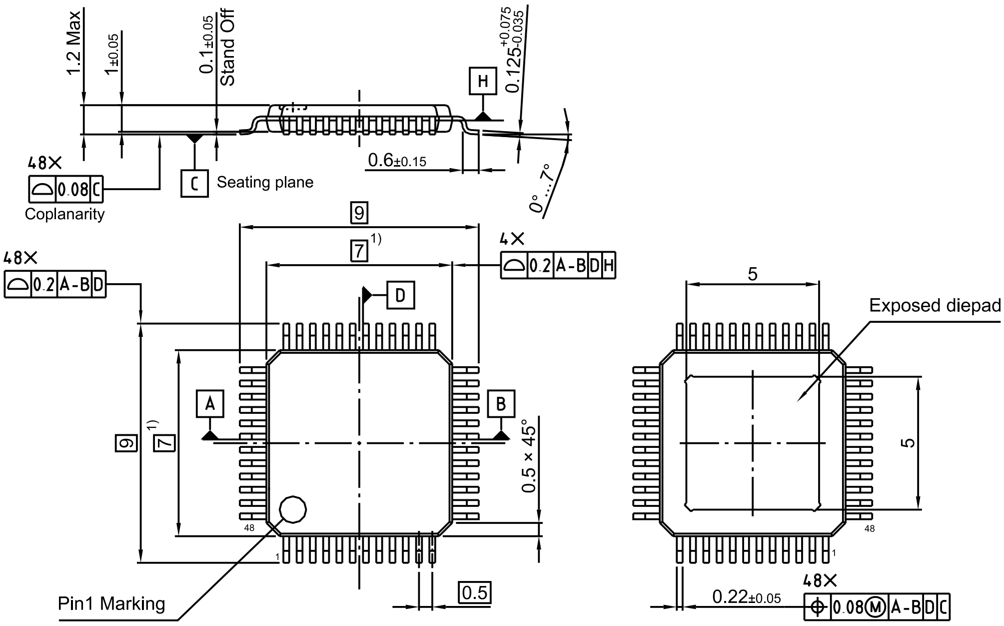
Table 74 VSD Overvoltage

V_S = 4.4 V to 28 V, Grade 0 devices: T_j = -40°C to +175°C, Grade 1 devices: T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VSD Overvoltage Rising	V_{SD_OV}	32	-	38	V	[1]	P_BDRV_08_01
VSD Overvoltage Hysteresis	$V_{SD\_OV\_hyst}$	1.3	1.9	2.5	V	[1]	P_BDRV_08_02
VSD Overvoltage Filter Time	$t_{VSD\_OV\_filt}$	10	12	14	µs	[1]	P_BDRV_08_03

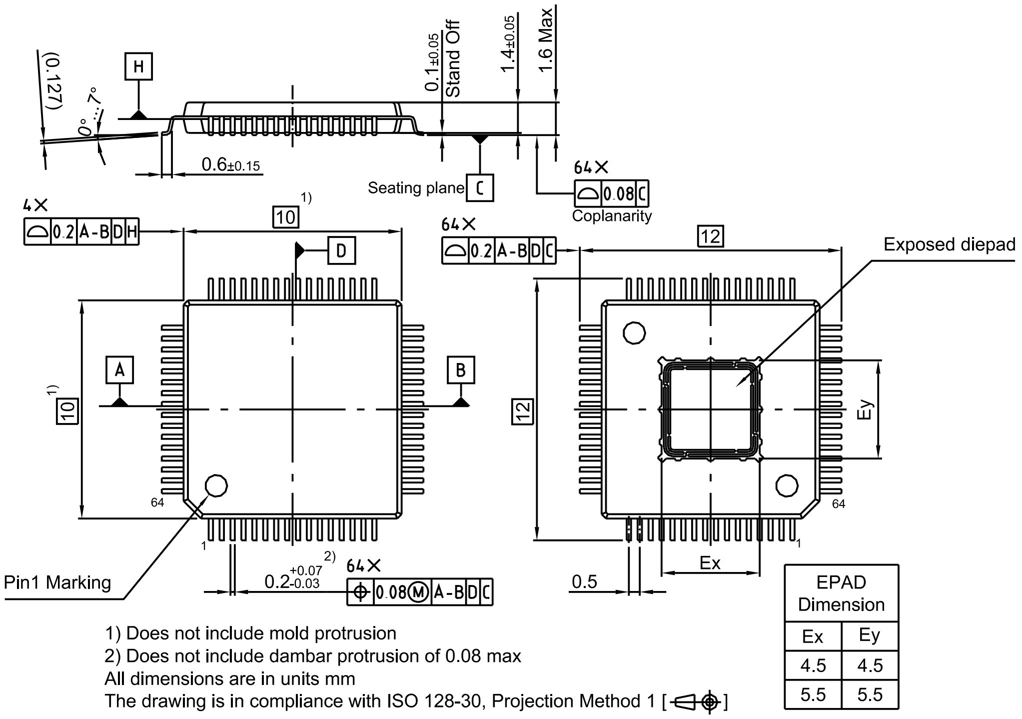
1) Not subject to production test, specified by design

27 Package information



1) Does not include plastic or metal protrusion of 0.25 Max per side
2) Exposed pad for soldering purpose
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊲⊕]
Drawing according to ISO 8015, general tolerances ISO 2769-mk

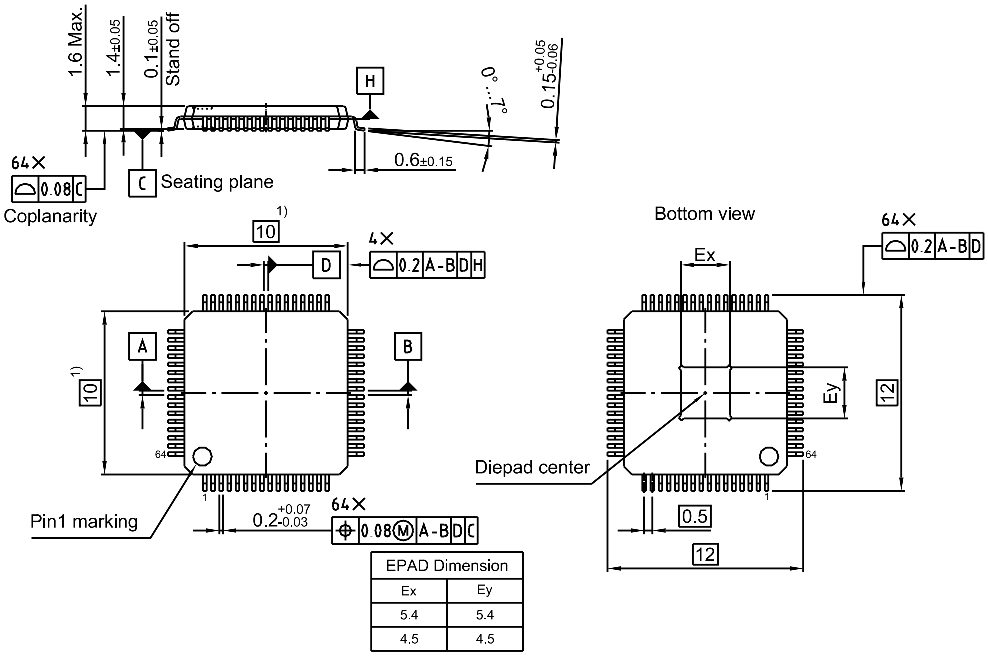
Figure 46 PG-TQFP-48-10



EPAD Dimension	
Ex	Ey
4.5	4.5
5.5	5.5

1) Does not include mold protrusion
2) Does not include dambar protrusion of 0.08 max
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊲⊕]

Figure 47 PG-LQFP-64-28



EPAD Dimension	
Ex	Ey
5.4	5.4
4.5	4.5

1) Does not include plastic or metal protrusion of 0.25 max. per side
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊲⊕]
Drawing according to ISO 8015, general tolerances ISO 2768-mK

Figure 48 PG-LQFP-64-31

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

28 Abbreviations

The following acronyms and terms are used within this document. List see in **Table 75**.

Table 75 Acronyms

Acronyms	Name
100TP	100 Time Programmable
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
ASIL	Automotive Safety Integrity Level
BEMF	Back Electro Magnetic Force
CAN	Controller Area Network
CP	Charge Pump for MOSFET driver
DMA	Direct Memory Access
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read Only Memory
FS	Functional Safety
FSM	Finite State Machine
GPIO	General Purpose Input Output
HiZ	High impedance
IEN	Interrupt Enable
LDO	Low DropOut voltage regulator
LOW	Long Open Window (for WDT)
LSB	Least Significant Bit
LQFP	Low profile Quad Flat Package
MCTRL	Motor control
MCU	Micro Controller Unit
MPU	Memory Protection Unit
MRST	Master Receive Slave Transmit
MSB	Most Significant Bit
MTSR	Master Transmit Slave Receive
N-FET	N-channel Field Effect Transistor
NMI	Non-Maskable Interrupt
NVIC	Nested Vector Interrupt Controller
NVM	Non-Volatile Memory
OSC	Oscillator
OT	Overtemperature
OTP	One Time Programmable
PBA	Peripheral Bridge
PC	Program Counter

Table 75 Acronyms (cont'd)

Acronyms	Name
PD	Pull Down
PLL	Phase Locked Loop
PMU	Power Management Unit
PPB	Private Peripheral Bus
PSRAM	Program Static Random Access Memory
PSW	Program Status Word
PU	Pull Up
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read Only Memory
SCB	Short Circuit to Battery
SCG	Short Circuit to Ground
SECDED	Single Error Correction Double Error Detection
SFR	Special Function Register
SoC	System on Chip
SOW	Short Open Window (for WDT)
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSO	Safe Switch Off (path)
SWD	Arm® Serial Wire Debug
TAP	Test Access Port (for test and debug)
TCCR	Temperature Compensation Control Register
TMS	Test Mode Select
TSD	Thermal Shut Down
TQFP	Thin Quad Flat Package
UART	Universal Asynchronous Receiver Transmitter
UV	Undervoltage
VBG	Voltage reference Band Gap
VCO	Voltage Controlled Oscillator
WDT	Watchdog timer in SCU-DM

29 Revision history

Revision	Date	Changes
Rev. 1.1	2023-06-19	Updated P_GEN_10_13
Rev. 1.0	2023-05-15	Initial version

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